TEKTRONIX®

~~WAYNE Auth~~

4012

COMPUTER DISPLAY TERMINAL

SERVICE

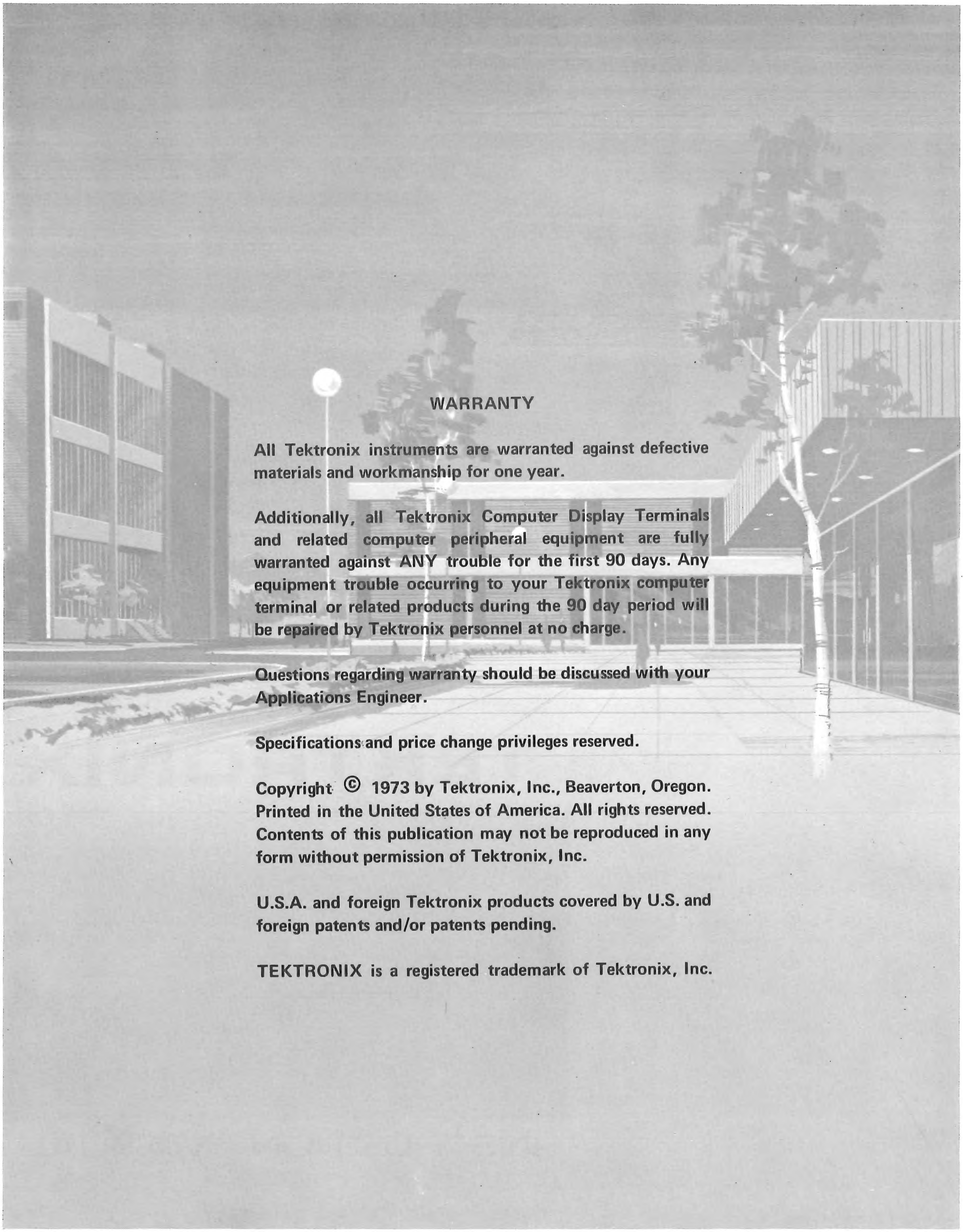
INSTRUCTION MANUAL

Tektronix, Inc.
P.O. Box 500
Beaverton, Oregon 97005

Serial Number ____________________

070-1461-00

773



WARRANTY

All Tektronix instruments are warranted against defective materials and workmanship for one year.

Additionally, all Tektronix Computer Display Terminals and related computer peripheral equipment are fully warranted against ANY trouble for the first 90 days. Any equipment trouble occurring to your Tektronix computer terminal or related products during the 90 day period will be repaired by Tektronix personnel at no charge.

Questions regarding warranty should be discussed with your Applications Engineer.

Specifications and price change privileges reserved.

TABLE OF CONTENTS

Fig. 1-1. 4012 Computer Display Terminal.

INSTALLATION AND OPERATION

This manual is a part of the following set of documents which describe the 4012 Computer Display Terminal:

4012 USERS MANUAL, Tektronix Part No. 070-1460-00.

Contents—An explanation of how to operate and program the Terminal.

4012 SERVICE MANUAL, Tektronix Part No. 070-1461-00.

Contents—A comprehensive explanation of the Terminal. It includes operation, characteristics, servicing, adjustment, circuit diagrams, circuit descriptions, and parts lists.

Optional items used with the Terminal are explained in separate manuals.

Introduction

The Computer Display Terminal interfaces between man and computer by permitting inputs through an integral keyboard and providing a display (alphanumeric or graphic) of computer output data. In addition, the Terminal can relay data bi-directionally between peripheral devices and a computer. An Interface Unit must be installed in the Terminal and connected to the computer — either directly or through a modem (modulator-demodulator)—to permit information interchange. Copies can be made of terminal displays, via a Hard Copy Unit.

INSTALLATION

General

The two main sections of the Terminal are the pedestal and the display unit. The pedestal section provides support for the display unit, and contains the power supply, control circuits, and optional circuits. The display unit contains the keyboard, the display storage CRT, and related circuits.

Desk-Mounting the Display Unit

The display unit and pedestal are connected only by a cable during shipment. Desk-mounting consists of simply setting the display unit on a desk or other surface. The pedestal can be placed as far as four feet away from the display unit. The air vents on the bottom and back should be kept free of obstructions. Note that if the base (leg assembly) is removed from the pedestal, the feet should be unscrewed from the base and inserted into the bottom of the pedestal to permit air flow into the bottom vents. However, make certain that the base is re-installed before the display unit is again placed on the pedestal.

If the display unit has been mounted on the pedestal, desk-mounting consists of reversing the pedestal-mounting procedure and observing the instructions which have just been outlined.

Pedestal-Mounting the Display Unit

Mounting of the display unit on the pedestal is best accomplished by two people. It includes the following steps:

1. If the Terminal has previously been used in a desk top configuration, the base (leg assembly) may have been removed from the pedestal and the feet installed directly into the bottom of the pedestal. In that event, put the feet back on the base, and fasten the base to the bottom of the pedestal.

2. Lift the display unit over the pedestal as shown in Fig. 1-2.

3. Feed the cable down into the storage bin as far as possible, while lowering the display unit into place. Then double the cable back and forth in the storage bin as lowering of the display unit continues.

4. There is a retaining strip on the bottom of the display unit. Slide it over the back edge of the pedestal top. Install four machine screws up through the pedestal top to fasten the display unit in place.

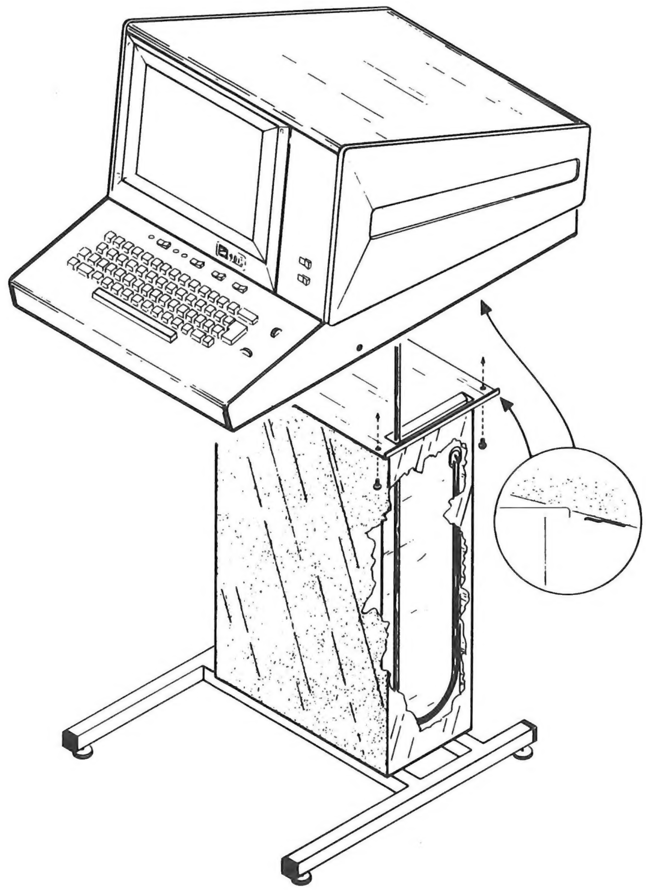


Fig. 1-2. Display Unit Mounting.

5. Adjust the four feet to a convenient position, and secure the lock nuts.

Pedestal Access

The pedestal is equipped with a hinged front cover. The upper section can be loosened and swung down to permit access to the minibus, into which the Terminal Control cards, interface cards and optional accessory cards are installed. Lowering of the top half permits access to the Terminal strap options without exposing dangerous voltages. The cover must be removed completely for access to the low voltage power supply, and to the line voltage transformer and fuse connections. The lower section of the cover has the line fuse installed in it, providing an automatic interlock when the front cover is fully removed.

WARNING

Dangerous voltages exist in the lower section of the pedestal when the line cord is connected. Servicing should be done only by qualified technicians.

Strappable Options

Strappable options on circuit cards in the pedestal should be placed in the desired position upon installation. Refer to Table 2-13 for details.

Interfacing

Connect the Interface Unit to the computer or modem, as appropriate. The Interface Unit is installed in the pedestal section of the Terminal and interconnecting cable(s) and plug(s) egress through the back of the pedestal unit. The configuration varies with the type of Interface Unit. The standard Terminal contains a Data Communication Interface No. 021-0065-00. The Optional Data Communication Interface No. 021-0074-00 or the TTY Port Interface may be supplied as options in place of the standard Data Communication Interface. Refer to the appropriate Interface documentation for specific installation instructions.

Optional Accessories

Refer to the documentation on the specific accessory for installation instructions.

Operating Power

The Terminal is intended to be operated from a single-phase power source which has one of its current-carrying conductors (the neutral conductor) at ground (earth) potential. Operation from other power sources where both current-carrying conductors are live with respect to ground (such as phase-to-phase on a multi-phase system, or across the legs of a 117-234 V single-phase three-wire system) is not recommended, as only the line conductor has over-current (fuse) protection within the instrument.

The Terminal is provided with a three-wire power cord with a three-terminal polarized plug for connection to the power source. The grounding terminal of the plug is directly connected to the instrument frame as recommended by national and international safety codes. Color coding of cord conductors follows the National Electrical Code (ANSI C1-1968) which specifies Line as Black, Neutral as White, Safety Earth or Ground as Green with a yellow stripe (or solid green).

The Terminal can be operated from either 110 or 220-volt nominal line voltage source. A clip-in fuse and a jumper arrangement on the transformer permit the Ter-

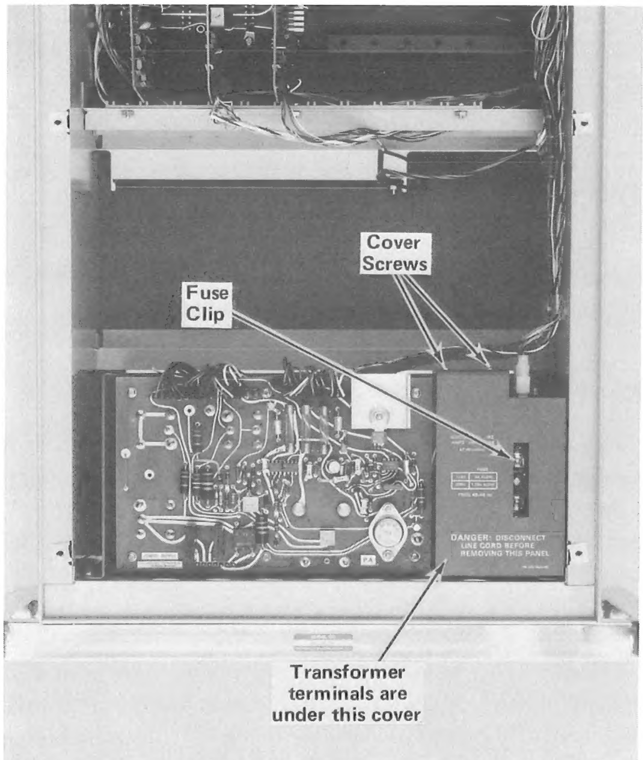


Fig. 1-3. Transformer terminals and fuse clip locations. (The fuse is contained on the pedestal front cover.)

minal to be modified to suit the supply. The fuse is mounted on the inside of the pedestal front cover, providing a cover interlock. The transformer and fuse clip are located in the bottom-right of the pedestal, as shown in Fig. 1-3. Fuse size is indicated on the transformer shield, and the wiring instructions are contained on the inside of the front cover. Wiring instructions are repeated in Fig. 1-4 for convenience. Fuse size is 2 A slo-blo for 110-volt operation and 1.25 A slo-blo for 220-volt operation. When changing fuses, the fuse should be pushed (rather than pulled) through the fuse holder. Line frequency may be between 48 and 440 Hz.

WARNING

Dangerous potentials exist in the lower section of the pedestal. Disconnect the Terminal from the power source before changing transformer connections.

INDICATORS AND CONTROLS

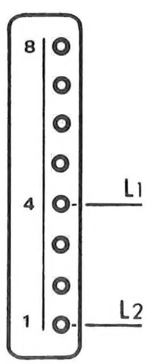
General

With the exception of the Power switch, all operator controls and indicators are located on the display unit. The Power switch is located on the upper right corner of the pedestal, immediately below the display unit. The Hard Copy Intensity adjustment knob is on the right side of the display unit.

Indicators

Power lamp — Illuminated by the +5 V supply when the Power switch is turned on.

Indicator 1
Indicator 2 — Multiple use lamps whose functions are determined by the accessories and optional equipment used with the Terminal. Connections to the lamp are made via the minibus. Low signals are required to light the lamps.



LINE CORD ALWAYS ATTACHED TO 1 & 4

JUMPER ARRANGEMENT

VOLTAGE ± 10%	100	115	120	200	220	230	240
TERMINAL NO.	1-8 4-5	1-2 3-4	1-7 4-6	5-8	5-7	2-3	6-7
	TWO JUMPERS REQUIRED			ONE JUMPER REQUIRED			

Fig. 1-4. Transformer terminals and jumper arrangement.

Switches

Power — Applies power to the Terminal. Located at the top-right corner on the front of the pedestal.

LOCAL/LINE — A two-position rocker switch. LOCAL position isolates the Terminal from the computer and permits keyboard inputs to be displayed or otherwise executed by the Terminal. LINE position permits communication with the computer, and keyboard inputs are not displayed or otherwise executed by the Terminal unless echoing is being done by the Interface Unit, modem, or computer.

Switch 1
Switch 2
Switch 3
Switch 4 — Two-position rocker switches whose functions are determined by the accessories and optional equipment used with the Terminal. Switch 1 and Switch 2 make connection via the minibus. Switches 3 and 4 make connection through wires and pin connectors which are fastened beneath a cable clamp on the right side within the pedestal.

MAKE COPY Switch — If a Hard Copy Unit is attached to the Terminal, the switch initiates making of a hard copy of the Terminal display.

Adjustments

Hard Copy Intensity — An adjustment knob located on the right side of the Display Unit. For hard copy operation, turn the control up to the point where the Hard Copy Unit scanning signal stores on the Terminal screen, then back off the adjustment to a point just below the storing level.

Spare Potentiometer — Adjustment knob located underneath the right side of the display unit. For use with accessory devices. Connection to the potentiometer is via the plug which is stored on J34 on the motherboard in the pedestal.

Thumbwheels

These are located on the right side of the keyboard section. They position the crosshair cursor that is displayed in GIN (Graphic Input) Mode.

Character Keys

Keyboard Entry. The keyboard shown in Fig. 1-5 is equipped to perform as an input for ASCII or TTY codes. Lower case letters, grave accent (\`), opening brace ({), broken vertical line (¦), and tilde (~) cannot be transmitted when the TTY LOCK key is depressed, regardless of the position of the shift key.

Repeat Entries. Character transmission occurs when a key is pressed. If the key is held down, a one-half second (approximate) delay occurs, after which the character is repeatedly entered at a 10 Hz rate. If CTRL or SHIFT is used with a character key, the originally selected code continues to be transmitted as long as the character key is held down, even if CTRL or SHIFT is subsequently released.

Control Keys

The following keys do not directly enter characters for transmission, but control operation of the keyboard or Terminal. Some of them are used independently, while others are used in combination with other control keys or character keys.

RESET/PAGE — Pressed alone, it performs a PAGE function. It erases the CRT, resets to Alpha Mode and Home position, resets to Margin Ø and cancels Echoplex Suppression. Pressed while SHIFT is held down, it creates a HOME function, resetting the Terminal to initial status; no erase occurs.

CTRL — Causes letter keys to transmit control characters if CTRL is held down before the letter key is pressed. It may be used in conjunction with SHIFT and a character key.

Fig. 1-5. 4012 Keyboard.

SHIFT — Used alone, it resets the Terminal from Hold to View status. It causes some keys to enter a shifted character if held down while the character key is pressed. It is also used in combination with CTRL and some letter keys for entering control characters.

TTY LOCK — Causes letter keys to transmit upper case letters, regardless of position of SHIFT key. TTY LOCK also inhibits transmission of the following:

` { | ~

BREAK — Generates a $\overline{\text{BREAK}}$ signal, which is sent to the interface unit. Any resulting interrupt signal is interface dependent.

Control Character Inputs

Control characters are input at the keyboard as listed in Table 1-1, regardless of TTY selection. The CTRL key or CTRL and SHIFT keys must be held down while the letter key is being entered, as indicated in the listing.

TABLE 1-1

Control Characters versus Keyboard Equivalents

Control Character	Keyboard Entry	Control Character	Keyboard Entry
ACK	CTRL F	FS	CTRL SHIFT L
BEL	CTRL G	GS	CTRL SHIFT M
BS	BACK SPACE or CTRL H	HT	TAB or CTRL I
CAN	CTRL X	LF	LF or CTRL J
CR	RETURN or CTRL M	NAK	CTRL U
DC1	CTRL Q	NUL	CTRL SHIFT P
DC2	CTRL R	RS	CTRL SHIFT N
DC3	CTRL S	SI	CTRL O
DC4	CTRL T	SO	CTRL N
DLE	CTRL P	SOH	CTRL A
EM	CTRL Y	STX	CTRL B
ENQ	CTRL E	SUB	CTRL Z
EOT	CTRL D	SYN	CTRL V
ESC	ESC or CTRL SHIFT K	US	CTRL SHIFT O
ETB	CTRL W	VT	CTRL K
ETX	CTRL C		
FF	CTRL L		

OPERATING MODES

General

Normal operation of the Terminal is achieved with the keyboard LOCAL/LINE switch at LINE position. The following operations are then possible:

Transmitting—Coded data is transmitted to the computer as entered at the keyboard.

Receiving—Alpha Mode causes alphanumeric characters to be written as received; control characters are executed as received; Terminal goes into a reduced intensity status (Hold) after approximately 90 seconds of inactivity; Terminal returns to View status upon keyboard entry or upon receipt of data from the computer. Graph Mode causes received data to be interpreted as specific addresses for the X and Y registers within the Terminal, resulting in moving the display unit beam to specific positions; the basic address positions are shown in Fig. 1-6. Control characters are executed as received.

Interactive—Graphic Input (GIN) Mode causes the Terminal to automatically send its status or the address of the display beam to the computer in response to commands from the computer. A crosshair cursor may be displayed in GIN Mode as a preparatory status.

Local operation occurs when the keyboard LOCAL/LINE switch is placed in the LOCAL position. The Terminal is then isolated from the computer, and keyboard entries are displayed or otherwise executed by the Terminal.

The Terminal has a Hard Copy Mode that permits a hard copy reproduction of the display to be made if a Hard Copy Unit is connected to the Terminal. The mode can be initiated by computer command, by a MAKE COPY key on the Terminal keyboard, or by a switch on the Hard Copy Unit.

Transmitting

If the keyboard switch is at LINE position, data entered at the keyboard is transmitted in coded form to the computer. The ASCII character set and its accompanying code is shown in Fig. 1-7.

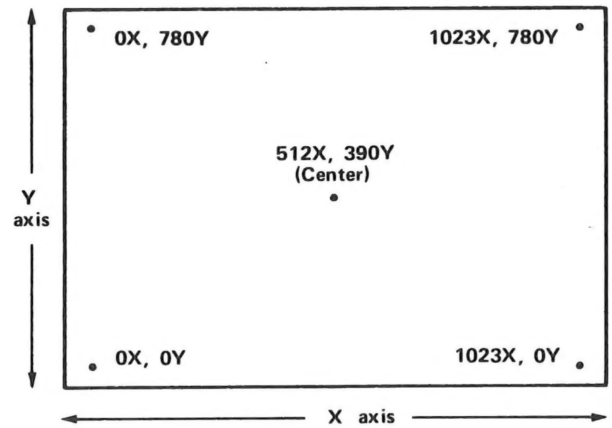


Fig. 1-6. Basic address positions on the display screen.

The TTY LOCK key locks out ` { ¦ ~ and lower case letters. The TTY LOCK key affects the keyboard transmission circuits, not the receiving circuits.

The keyboard generates an eighth bit which is always either high or low, depending upon a strap option in the keyboard. This may be sent as set at the keyboard, or may be determined by the interface unit.

Receiving

General. The Terminal receiving circuits are essentially isolated from the keyboard and transmitting circuits while the keyboard switch is at LINE position. Data is then received as a result of transmission from the computer, including data being echoed by the computer or modem. However, data entered at the keyboard is applied to the receiving circuits if an ECHO signal is being asserted by the interface unit. ECHO is controlled by a switch or a strap option, depending upon the type of interface. The ECHO signal creates a situation referred to as echoplexing.

The Terminal response to signals thus received is essentially the same in either case, and depends upon the operating mode.

Alpha Mode. The Alpha Mode is the initial condition of the receiving circuits. In addition, it occurs in response to receiving a US, CR, or ESC FF. It is also initiated by entering PAGE or SHIFT RESET at the keyboard. A pulsating cursor indicates the writing position of the next character. Alphanumeric characters are written on the display screen, essentially as shown in Fig. 1-7 or 1-8. Note that the TTY LOCK key has no control over incoming data, and any character can be written in response to appropriate

ASCII/TTY CODE CHART
(shaded areas are not included in TTY Code)

BITS B4	B3	B2	B1	B7 Ø B6 Ø B5 Ø	B7 Ø B6 Ø B5 1	B7 Ø B6 1 B5 Ø	B7 Ø B6 1 B5 1	B7 1 B6 Ø B5 Ø	B7 1 B6 Ø B5 1	B7 1 B6 1 B5 Ø	B7 1 B6 1 B5 1
				CONTROL		HIGH X & Y GRAPHIC INPUT		LOW X GRAPHIC INPUT		LOW Y GRAPHIC INPUT	
Ø	Ø	Ø	Ø	NUL Ø	DLE 16	SP 32	Ø 48	@ 64	P 8Ø	` 96	p 112
Ø	Ø	Ø	1	SOH 1	DC1 17	! 33	1 49	A 65	Q 81	a 97	q 113
Ø	Ø	1	Ø	STX 2	DC2 18	" 34	2 5Ø	B 66	R 82	b 98	r 114
Ø	Ø	1	1	ETX 3	DC3 19	# 35	3 51	C 67	S 83	c 99	s 115
Ø	1	Ø	Ø	EOT 4	DC4 2Ø	$ 36	4 52	D 68	T 84	d 1ØØ	t 116
Ø	1	Ø	1	ENQ 5	NAK 21	% 37	5 53	E 69	U 85	e 1Ø1	u 117
Ø	1	1	Ø	ACK 6	SYN 22	& 38	6 54	F 7Ø	V 86	f 1Ø2	v 118
Ø	1	1	1	BEL 7 BELL	ETB 23	' 39	7 55	G 71	W 87	g 1Ø3	w 119
1	Ø	Ø	Ø	BS 8 BACK SPACE	CAN 24	(4Ø	8 56	H 72	X 88	h 1Ø4	x 12Ø
1	Ø	Ø	1	HT 9	EM 25	) 41	9 57	I 73	Y 89	i 1Ø5	y 121
1	Ø	1	Ø	LF 1Ø LINE FEED	SUB 26	* 42	: 58	J 74	Z 9Ø	j 1Ø6	z 122
1	Ø	1	1	VT 11	ESC 27	+ 43	; 59	K 75	[91	k 1Ø7	{ 123
1	1	Ø	Ø	FF 12	FS 28	, 44	< 6Ø	L 76	\ 92	l 1Ø8	¦ 124
1	1	Ø	1	CR 13 RETURN	GS 29	– 45	= 61	M 77	] 93	m 1Ø9	} 125
1	1	1	Ø	SO 14	RS 3Ø	. 46	> 62	N 78	^ 94	n 11Ø	~ 126
1	1	1	1	SI 15	US 31	/ 47	? 63	O 79	_ 95	o 111	127 RUBOUT (DEL)

Fig. 1-7. ASCII Code Chart.

code and character set selection. Space causes spacing only. DEL causes neither spacing nor writing. Control characters and control character sequences cause effects as listed in Table 2-1. Optional accessories may respond to other commands or sequences as determined by the optional accessory. Refer to Table 2-2 for a listing of Alpha Mode specifications.

Graph Mode. Control character GS puts the Terminal in Graph Mode. Then the Terminal draws vectors (either written or unwritten) in response to graphic address inputs as explained in Tables 2-4 and 2-5. The Terminal can still respond to control characters and control character sequences as explained in Table 2-1. Graph Mode ends and Alpha Mode occurs upon receipt of control characters US, CR, or control character sequence ESC FF. Graph Mode also ends upon receipt of ESC SUB, which sets GIN Mode and displays the crosshair cursor. Graph Mode can also be ended by pressing PAGE or SHIFT RESET at the keyboard. Refer to Table 2-3 for Graph Mode specifications.

Interactive

GIN Mode. GIN Mode occurs in response to receipt of ESC ENQ at any time the Terminal is "on line". It also occurs in response to an ESC SUB, which turns on the crosshair cursor. ESC SUB should not be entered at the keyboard while "on line", because immediate and erroneous transmission may occur. Receipt of ESC ENQ while in Alpha Mode results in immediate transmission of the Terminal status and the address of the point at the lower left corner of the Alpha cursor. CR or CR and EOT will automatically be transmitted immediately after the address, if selected by a strap option on TC-2. (EOT cannot be sent without CR.) Echoplexing is suppressed during GIN Mode. GIN Mode ends upon completion of transmission. If CR is transmitted during GIN Mode and is echoed by the computer, the Terminal will return to full Alpha Mode upon completion of the transmission. If CR is not echoed, the Terminal must be reset by one of the following before character writing can occur: BEL, BS, CR, ESC ETB, ESC FF, HT, LF, US, or VT. Note that if CR is echoed, or if any command affecting the display position is sent to the Terminal, it will cause the cursor to move away from the position that was referenced in GIN Mode; use BEL or US if the display position is to be left undisturbed.

Receipt of ESC ENQ while in Graph Mode also causes GIN Mode, sending the Terminal status and address of the Graph Mode beam position to the computer. The computer or modem may not echo GIN Mode data back to the Terminal if Graph Mode and beam position are to be retained after an ESC ENQ. (CR echoed will reset the Terminal to Alpha Mode, and will move the cursor to the left margin; echoing the status and address bytes will change the beam address to a point different from that sent to the computer.) GIN Mode ends automatically upon completion of transmission, and the Terminal returns to full Graph Mode if CR is not echoed.

Receipt of ESC SUB sets GIN Mode and turns on the crosshair cursor as a preparatory step in transmitting an address to the computer. The thumbwheels (located on the keyboard) can be used to position the crosshair cursor anywhere in the display area. The address at the crosshair intersection is sent to the computer in response to an ESC ENQ from the computer, or in response to entry of any keyboard character. The Terminal returns to full Alpha Mode upon completion of transmission if CR is sent and echoed. If CR is not echoed, one of the following must be sent before the Terminal can again write: BEL, BS, CR, ESC ETB, ESC FF, HT, LF, US, or VT. Refer to Table 2-6 for GIN Mode specifications.

Local

Operation with the LOCAL/LINE switch at LOCAL is much the same as just described for LINE operation. However, the following exceptions exist: (1) The Terminal is isolated from the computer; (2) data entered at the keyboard while in Alpha Mode results in writing or executing data at the Terminal; (3) data entered at the keyboard while in Graph Mode results in drawing vectors or executing control characters at the Terminal; (4) the crosshair cursor appears in response to CTRL SHIFT K and CTRL Z, and can be positioned by the thumbwheels — but it can only be removed by entering SHIFT RESET or PAGE.

FIRST-TIME OPERATION

This operation procedure is intended to acquaint a user with the operating features of the Terminal. It can also be used as a Terminal check-out procedure. Although the Terminal is not connected to a modem or computer, all modes are exercised. Computer echoing is simulated by a local echo feature. Responses are explained for all options.

Preliminary

The Terminal should not be connected to a power source, modem, or computer at this time.

WARNING

Dangerous voltage exists in the lower section of the pedestal. Servicing should be done by a qualified technician.

Line Voltage. If the Terminal is being initially installed, check that the line voltage agrees with the voltage written on the tag which is attached to the Terminal. If it does not, remove the front cover of the pedestal after removing the screws, and change the transformer wiring and fuse size so that they agree with the power source. Wiring instructions appear inside the pedestal cover; fuse sizes are written on the transformer cover plate. The tag information should be changed when the wiring is changed. Replace the front cover.

Power. Plug the power cord into the power source and turn the Terminal Power switch ON. The switch is located on the front at the top of the pedestal.

Power Lamp. Check that the Power lamp on the left of the keyboard illuminates, and the display screen becomes bright.

Data Transmission. With the keyboard switch at LINE, keyboard data is sent to the computer. It goes to the Terminal receiving circuits only if it is presented to them by one of the following methods: (1) Echoed by the computer or modem; (2) Echoed by the Terminal's interface unit.

With the keyboard switch at LOCAL, the Terminal is isolated from the computer; data entered at the keyboard is applied to the Terminal receiving circuits in a manner similar to that which occurs when the keyboard switch is at LINE and the interface unit is echoing data. LOCAL provides a dual advantage. It permits an evaluation of the data being transmitted by the keyboard, and at the same time tests the Terminal receiving circuits. For these reasons, LOCAL operation is used for most of this procedure. Differences between LOCAL and LINE operation are mentioned whenever they occur. *IT SHOULD BE KEPT IN MIND THAT THE KEYBOARD'S PRIMARY FUNCTION IS TO ACT AS A SOURCE FOR THE COMPUTER; THE RECEIVING CIRCUIT'S PRIMARY FUNCTION IS TO RESPOND TO DATA FROM THE COMPUTER: THE KEYBOARD IS SIMPLY BEING USED AS A SOURCE OF DATA FOR THE RECEIVING CIRCUITS WHILE IN LOCAL OPERATION.*

Initialization

Press the PAGE key to erase the display screen. The screen must be erased each time the Terminal is turned on. PAGE also selects Alpha Mode and places the beam at the upper-left corner of the display (Alpha Mode "home" position).

Alpha Mode

ASCII Character Transmission and Character Effect. Check that the TTY LOCK key is not actuated. If it is, press the key once to release the lock. Press each key in the keyboard cluster and note the effect. Most of them will cause unshifted character writing, permitting a check of the code being transmitted by the keyboard and a check of the dot pattern being presented by the character generator in the receiving circuits. Keys that are an exception to this are as follows:

PAGE/RESET—Causes no transmission. When pressed alone, it causes Alpha Mode to be selected, causes erasing and places the Alpha cursor to the top-left corner of the display (Alpha Mode "home" position). When pressed while the SHIFT key is held down, it initializes the Terminal without erasing it, selecting Alpha Mode "home" position, and resetting programmable circuits.

ESC—Transmits the control character ESC, which arms the Terminal circuits in anticipation of receiving one of certain subsequent characters. As an example, enter ESC and CTRL L, causing the control character FF to be transmitted. When FF is accepted by the receiving circuits after they have been armed by ESC, it causes the display to erase and the Alpha cursor to go home. FF alone cannot do it. (A complete listing of control character effects appears in Table 2-1.)

TAB—Transmits control character HT, which causes the cursor to move right one space.

CTRL—Has no effect as a single key entry. It causes the keyboard to transmit control characters when used with other keyboard keys. As an example, enter a G while the CTRL key is held down; it transmits the control character BEL, which causes the receiving circuits to ring the bell. As a second example, hold down CTRL and SHIFT and press M to transmit the control character GS. This switches the Terminal to Graph Mode, as evidenced by the absence of the Alpha cursor. Enter CTRL SHIFT O to transmit a US, which switches the Terminal back to Alpha Mode; the Alpha cursor will reappear.

SHIFT—Its only effect as a single key entry is to restore View condition, without otherwise affecting transmission or the receiving circuits. Wait until Hold status occurs. Then press SHIFT and note the effect. When SHIFT is used with other keys, it causes the shifted character to be transmitted as indicated on each key. When used with CTRL and certain other character keys, it causes transmission of control characters as listed in Table 1-1, and defined in the CTRL key explanation.

BACK SPACE—Transmits control character BS, causing the cursor to move back one space. Enter a space command and then press BACK SPACE and note the effect.

LF—Transmits the control character LF. At the receiving circuits, LF causes the Alpha cursor to move down to the next line. The cursor may also move to the left margin if the "LF EFFECT" strap option on TC-1 is at LF→CR position. Enter an LF and observe the results.

RETURN—Transmits the control character CR. At the receiving circuits, it causes the Alpha cursor to move to the left margin. There are two "left" margin positions. One is vertically aligned with the "home" position and is referred to as "Margin Ø". The second is near the horizontal center of the screen, and is referred to as "margin 1". Margin 1 is automatically selected each time the Terminal line-feeds past the 35th (last) line while Margin Ø exists. Margin Ø is selected when the Terminal line-feeds past the 35th line while Margin 1 exists, and is also selected when ESC FF is received or when PAGE or SHIFT RESET is entered at the keyboard. CR also causes a line feed to occur if the CR EFFECT strap on TC-1 is in the CR→LF position.

RUBOUT—This key sends the ASCII code for DEL. The receiving circuits accept it, but it causes no spacing, writing, or other obvious effect.

BREAK—Sends a break signal to the interface unit, which may then transmit a break signal to the computer. Has no effect upon the receiving circuits.

Automatic Line Feed and Carriage Return. By now, it probably has been noticed that the Terminal receiving circuits automatically perform a carriage return and line feed each time the last (74th) character in a line is written. If it hasn't been noticed, hold down a writing character key until a full line of characters is written, and observe the effect. Note that the Alpha Cursor returns to the effective margin position — Margin Ø or Margin 1.

Margins. Enter a PAGE command and note the cursor position at the left edge (Margin Ø) of the display. Hold the LF key down until the cursor disappears past the bottom of the display screen, and note that it re-appears at the top-center of the display, in Margin 1 position. Hold the LF key down until the cursor moves past the bottom of the display; it will re-appear at the top in Margin Ø position. *THE EFFECTIVE MARGIN CONDITION CHANGES EACH TIME THE DISPLAY LINE-FEEDS PAST THE LAST (35th) LINE.*

Again arrive at the Margin 1 position and enter several SP characters at the Space bar. Then press the RETURN key to send a CR to the receiving circuits. Note that the cursor returns to the effective margin position, in this case Margin 1. Now enter enough characters to space past the end of the line. Note that the cursor returns to Margin 1. *CR, RETURN, OR AUTOMATIC CARRIAGE RETURN SETS THE CURSOR BACK TO THE EFFECTIVE MARGIN POSITION.*

Press SHIFT RESET to set Margin Ø. Now enter characters until a line is fully written and an automatic line feed — carriage return occurs. Note that character writing ignores Margin 1 position or Margin 1 information while Margin Ø exists. *IF TWO-COLUMN FORMATTING IS TO OCCUR, MARGIN Ø INFORMATION MUST BE KEPT TO 36 CHARACTERS OR LESS.*

View/Hold. Wait about 90 seconds and note that the Terminal automatically enters a reduced intensity condition referred to as Hold. This condition prolongs tube life, and occurs in Alpha Mode only. *THEREFORE, THE TERMINAL SHOULD ALWAYS BE PLACED IN ALPHA MODE WHEN ENERGIZED, BUT NOT IN USE.*

TTY Character Transmission and Character Effects. The Terminal operation with TTY LOCK activated is essentially the same as for ASCII. The difference is that a truncated character set is available for transmission as illustrated in Fig. 1-7.

Place the TTY LOCK key in its active position. Now enter various letters and note that they write as upper case, regardless of the position of the SHIFT key.

Graph Mode

Press the SHIFT key and note the position of the Alpha Cursor. Then send GS (CTRL SHIFT M) to the receiving circuits and note that the Alpha cursor disappears. Send the address 383Y, 512X to place the beam near the center of the screen. The required bytes can be determined from Fig. 1-8 through 1-11. They equate to + DEL Ø @ in ASCII code. Enter + RUBOUT Ø @ at the keyboard. (RUBOUT transmits DEL.)

Unwritten Vector. No obvious results occur in response to the just-entered characters, because they make up the first address to be received after a GS, and the beam is blanked while the movement occurs.

Written Vector. Enter @ again. It will execute a second vector, which will be written. This vector appears as a dot near the center of the screen, since no change in position was commanded. (The @ contains the code for a Low X byte, which causes vector execution.) Now send the address for 32Y, 32X. This equates to SP DEL SP _ and is entered at the keyboard as Space RUBOUT Space _ to draw the vector. Note that nothing happens until the Low X (last) command is entered, but then a vector is drawn from the center to the lower left corner.

Resetting With US. Now go back to Alpha Mode without otherwise disturbing the receiving circuits, by sending a US to the Terminal. Do it by entering a CTRL SHIFT O at the keyboard. Note that the Alpha cursor appears with its lower left corner at the end of the vector, since US causes no change in the Terminal position-register contents.

Graph Memory. Send ten SP commands to the Terminal by pressing the keyboard Space bar. Note that the cursor moves away from the end of the vector. Put the Terminal back in Graph Mode by sending it a GS (CTRL SHIFT M). Then send the same Low X command as was last used, by again entering _ at the keyboard. The beam will move unseen back to the end of the vector because of the Graph Mode memory circuits. This can be confirmed by entering a second _ at the keyboard, to again send the Low X command to the receiving circuits. Note that the same Low X command as contained in the last address must be used, or the beam position will differ by the amount of difference between the two Low X bytes.

Resetting With CR. Now switch from Graph Mode to Alpha Mode by sending a CR to the receiving circuits. This can be done by pressing the RETURN key or entering a CTRL M at the keyboard. This places the Alpha cursor at the left margin. If the CR EFFECT strap on TC-1 is at CR, the cursor is placed in line with the last graphic position of the beam; if the strap is at CR→LF, the cursor is placed one line below the last graphic position.

Resetting With ESC FF. Send a GS to the receiving circuits by entering a CTRL SHIFT M at the keyboard. Enter two _ commands to confirm that the Terminal is back in Graph Mode, and is at the end of the drawn vector. Then send an ESC FF sequence to the receiving circuits. Do this by entering ESC and then CTRL L. Note that this erases the display, selects Alpha Mode, and homes the Alpha cursor. This can also be done locally by pressing the PAGE key, regardless of the position of the LOCAL/LINE switch.

Resetting With RESET. Send another GS (CTRL SHIFT M) to the receiving circuits, enter _ to return to the last graphic address, and then draw a vector to 32Y, 1023X. This translates to SP DEL ? _ which can be sent by entering Space RUBOUT ? _ at the keyboard. Now press the SHIFT and RESET keys at the keyboard. Note that the Alpha Mode is restored, and the Alpha cursor appears at the top left corner of the screen. No erasing occurs. This particular operation can only be accomplished from the keyboard. No program command equivalent to SHIFT RESET can be sent.

Shortened Addresses. The sequence in Table 1-2 illustrates the ability of the receiving circuits to respond to various graphic commands of less than four bytes. The missing bytes remain as sent in the last address which contained them. Table 2-5 specifies the minimum bytes that can be sent in any one situation.

View/Hold. The Hold feature is over-ridden while the Terminal is in Graphic Mode. *THE TERMINAL SHOULD ALWAYS BE RETURNED TO ALPHA MODE WHEN ENERGIZED, BUT NOT IN USE.*

TABLE 1-2

Shortened Address Illustration

Address & Comment	Send	
	ASCII	Keyboard
543Y, 543X. (Initial address; send 4 bytes.)	∅ DEL ∅ _	∅ RUBOUT ∅ _
543Y, 512X. (Lo X changes; send only Lo X.)	@	@
541Y, 512X. (Lo Y changes; send Lo Y, Lo X.)	} @	} @
29Y, 512X. (Hi Y changes; send Hi Y, Lo X.)	SP @	Space @
29Y, 0X. (Hi X changes; send Lo Y, Hi X, Lo X.)	} SP @	} Space @
543Y, 0X. (Hi Y and Lo Y change; send Hi Y, Lo Y, Lo X.)	∅ DEL @	∅ RUBOUT @
31Y, 543X. (Hi Y, Hi X, and Lo X change; send four bytes.)	SP DEL ∅ _	Space RUBOUT ∅ _

GIN Mode

Crosshair Cursor. Enter ESC and CTRL Z and note that a crosshair cursor appears. (If the horizontal thumbwheel is in either limit, the vertical line may be the only line to appear; with the vertical thumbwheel at the lower limit, the horizontal line may be the only line to appear. Move both thumbwheels out of their limits to present both lines.) Check that the cursor can be moved via the thumbwheels. Press any key except PAGE or SHIFT RESET and note that they have no effect. Press PAGE or SHIFT RESET and note that the crosshair cursor disappears and the Alpha cursor returns. *THE RECEIVING CIRCUITS ARE INSENSITIVE TO SIGNALS FROM THE KEYBOARD WHILE IN LOCAL WITH THE CROSSHAIR CURSOR DISPLAYED. IT SHOULD ALSO BE NOTED THAT THE CROSSHAIR CURSOR CANNOT BE CALLED INTO VIEW BY THE KEYBOARD WHILE ON LINE: IN NORMAL OPERATION, AN ESC SUB FROM THE COMPUTER COMMANDS IT TO APPEAR.*

GIN Mode Transmissions. These cannot be demonstrated with the keyboard switch at LOCAL position. Refer to the Operating Modes information at the beginning of this section, or refer to Table 2-6 for details concerning "on-line" GIN Mode operation.

View/Hold. The Hold feature is disabled while the crosshair cursor is displayed. *THEREFORE, THE TERMINAL SHOULD ALWAYS BE RESET TO ALPHA MODE WHEN ENERGIZED, BUT NOT IN USE, TO PROLONG TUBE LIFE.*

Hard Copy Mode

Connect a Hard Copy Unit to the Terminal and energize it. Switch the Terminal's LOCAL/LINE control to LOCAL. Enter a number of alphanumeric characters at the keyboard to create a display.

Transmit an ESC ETB signal to the receiving circuits by entering ESC and CTRL W at the keyboard. (Pressing the MAKE COPY button on the keyboard, or pressing the Copy button on the Hard Copy Unit will achieve the same effects.) A scanning bar should appear and scan the display. A few seconds after scanning is completed, the Hard Copy Unit should eject a hard copy of the display. If the paper is blank, or if information dropout occurs, the Hard Copy Intensity control on the right side of the Terminal may be set too low. On the other hand, if the scanning bar causes storing on the display, the Hard Copy Intensity control may be set too high. Readjust the control while copy making is occurring, selecting a point just below that where the scanning bar stores. Then press PAGE, enter more characters on the display, and make another copy. If the adjustment is made properly, a clear copy of the display should result.

COORDINATE CONVERSION CHART

Low Order X		X or Y Coordinate								Low Order Y	
ASCII	DEC.									DEC.	ASCII
@	64	0	32	64	96	128	160	192	224	96	`
A	65	1	33	65	97	129	161	193	225	97	a
B	66	2	34	66	98	130	162	194	226	98	b
C	67	3	35	67	99	131	163	195	227	99	c
D	68	4	36	68	100	132	164	196	228	100	d
E	69	5	37	69	101	133	165	197	229	101	e
F	70	6	38	70	102	134	166	198	230	102	f
G	71	7	39	71	103	135	167	199	231	103	g
H	72	8	40	72	104	136	168	200	232	104	h
I	73	9	41	73	105	137	169	201	233	105	i
J	74	10	42	74	106	138	170	202	234	106	j
K	75	11	43	75	107	139	171	203	235	107	k
L	76	12	44	76	108	140	172	204	236	108	l
M	77	13	45	77	109	141	173	205	237	109	m
N	78	14	46	78	110	142	174	206	238	110	n
O	79	15	47	79	111	143	175	207	239	111	o
P	80	16	48	80	112	144	176	208	240	112	p
Q	81	17	49	81	113	145	177	209	241	113	q
R	82	18	50	82	114	146	178	210	242	114	r
S	83	19	51	83	115	147	179	211	243	115	s
T	84	20	52	84	116	148	180	212	244	116	t
U	85	21	53	85	117	149	181	213	245	117	u
V	86	22	54	86	118	150	182	214	246	118	v
W	87	23	55	87	119	151	183	215	247	119	w
X	88	24	56	88	120	152	184	216	248	120	x
Y	89	25	57	89	121	153	185	217	249	121	y
Z	90	26	58	90	122	154	186	218	250	122	z
[	91	27	59	91	123	155	187	219	251	123	{
\	92	28	60	92	124	156	188	220	252	124	|
]	93	29	61	93	125	157	189	221	253	125	}
∧	94	30	62	94	126	158	190	220	254	126	~
_	95	31	63	95	127	159	191	223	255	127	RUBOUT (DEL)
DEC. →		32	33	34	35	36	37	38	39		
ASCII →		SP	!	"	#	$	%	&	'		
		High Order X & Y									

Fig. 1-8. Coordinate conversion chart, part 1 of 4. INSTRUCTIONS: Find coordinate value in body of chart; follow that column to bottom of chart to find decimal value or ASCII character which represents the High Y or High X byte; go to the right in the row containing the coordinate value to find the Low Y byte, or go to the left to find the Low X byte. EXAMPLE: 200Y, 38X equals 38 104 33 80 in decimal code and equals & h ! P in ASCII code.

COORDINATE CONVERSION CHART
(cont)

Low Order X		X or Y Coordinate								Low Order Y	
ASCII	DEC.									DEC.	ASCII
@	64	256	288	320	352	384	416	448	480	96	`
A	65	257	289	321	353	385	417	449	481	97	a
B	66	258	290	322	354	386	418	450	482	98	b
C	67	259	291	323	355	387	419	451	483	99	c
D	68	260	292	324	356	388	420	452	484	100	d
E	69	261	293	325	357	389	421	453	485	101	e
F	70	262	294	326	358	390	422	454	486	102	f
G	71	263	295	327	359	391	423	455	487	103	g
H	72	264	296	328	360	392	424	456	488	104	h
I	73	265	297	329	361	393	425	457	489	105	i
J	74	266	298	330	362	394	426	458	490	106	j
K	75	267	299	331	363	395	427	459	491	107	k
L	76	268	300	332	364	396	428	460	492	108	l
M	77	269	301	333	365	397	429	461	493	109	m
N	78	270	302	334	366	398	430	462	494	110	n
O	79	271	303	335	367	399	431	463	495	111	o
P	80	272	304	336	368	400	432	464	496	112	p
Q	81	273	305	337	369	401	433	465	497	113	q
R	82	274	306	338	370	402	434	466	498	114	r
S	83	275	307	339	371	403	435	467	499	115	s
T	84	276	308	340	372	404	436	468	500	116	t
U	85	277	309	341	373	405	437	469	501	117	u
V	86	278	310	342	374	406	438	470	502	118	v
W	87	279	311	343	375	407	439	471	503	119	w
X	88	280	312	344	376	408	440	472	504	120	x
Y	89	281	313	345	377	409	441	473	505	121	y
Z	90	282	314	346	378	410	442	474	506	122	z
[	91	283	315	347	379	411	443	475	507	123	{
\	92	284	316	348	380	412	444	476	508	124	|
]	93	285	317	349	381	413	445	477	509	125	}
∧	94	286	318	350	382	414	446	478	510	126	~
_	95	287	319	351	383	415	447	479	511	127	RUBOUT (DEL)
DEC. →		40	41	42	43	44	45	46	47		
ASCII →		(	)	*	+	,	—	.	/		
		High Order X & Y									

Fig. 1-9. Coordinate conversion chart, part 2 of 4. (Refer to part 1 for interpretation instructions.)

COORDINATE CONVERSION CHART
(cont)

Low Order X		X or Y Coordinate								Low Order Y	
ASCII	DEC.									ASCII	DEC.
@	64	512	544	576	608	640	672	704	736	`	96
A	65	513	545	577	609	641	673	705	737	a	97
B	66	514	546	578	610	642	674	706	738	b	98
C	67	515	547	579	611	643	675	707	739	c	99
D	68	516	548	580	612	644	676	708	740	d	100
E	69	517	649	581	613	645	677	709	741	e	101
F	70	518	550	582	614	646	678	710	742	f	102
G	71	519	551	583	615	647	679	711	743	g	103
H	72	520	552	584	616	648	680	712	744	h	104
I	73	521	553	585	617	649	681	713	745	i	105
J	74	522	554	586	618	650	682	714	746	j	106
K	75	523	555	587	619	651	683	715	747	k	107
L	76	524	556	588	620	652	684	716	748	l	108
M	77	525	557	589	621	653	685	717	749	m	109
N	78	526	558	590	622	654	686	718	750	n	110
O	79	527	559	591	623	655	687	719	751	o	111
P	80	528	560	592	624	656	688	720	752	p	112
Q	81	529	561	593	625	657	689	721	753	q	113
R	82	530	562	594	626	658	690	722	754	r	114
S	83	531	563	595	627	659	691	723	755	s	115
T	84	532	564	596	628	660	692	724	756	t	116
U	85	533	565	597	629	661	693	725	757	u	117
V	86	534	566	598	630	662	694	726	758	v	118
W	87	535	567	599	631	663	695	727	759	w	119
X	88	536	568	600	632	664	696	728	760	x	120
Y	89	537	569	601	633	665	697	729	761	y	121
Z	90	538	570	602	634	666	698	730	762	z	122
[	91	539	571	603	635	667	699	731	763	{	123
\	92	540	572	604	636	668	700	732	764	|	124
]	93	541	573	605	637	779	701	733	765	}	125
^	94	542	574	606	638	670	702	734	766	~	126
_	95	543	755	607	639	671	703	735	767	RUBOUT (DEL)	127
DEC →		48	49	50	51	52	53	54	55		
ASCII →		0	1	2	3	4	5	6	7		
		High Order X & Y									

Fig. 1-10. Coordinate conversion chart, part 3 of 4. (Refer to part 1 for interpretation instructions.)

COORDINATE CONVERSION CHART

(cont)

Low Order X		X or Y Coordinate								Low Order Y	
ASCII	DEC.									DEC.	ASCII
@	64	768	800	832	864	896	928	960	992	96	`
A	65	769	801	833	865	897	929	961	993	97	a
B	66	770	802	834	866	898	930	962	994	98	b
C	67	771	803	835	867	899	931	963	995	99	c
D	68	772	804	836	868	900	932	964	996	100	d
E	69	773	805	837	869	901	933	965	997	101	e
F	70	774	806	838	870	902	934	966	998	102	f
G	71	775	807	839	871	903	935	967	999	103	g
H	72	776	808	840	872	904	936	968	1000	104	h
I	73	777	809	841	873	905	937	969	1001	105	i
J	74	778	810	842	874	906	938	970	1002	106	j
K	75	779	811	843	875	907	939	971	1003	107	k
L	76	780	812	844	876	908	940	972	1004	108	l
M	77	781	813	845	877	909	941	973	1005	109	m
N	78	782	814	846	878	910	942	974	1006	110	n
O	79	783	815	847	879	911	943	975	1007	111	o
P	80	784	816	848	880	912	944	976	1008	112	p
Q	81	785	817	849	881	913	945	977	1009	113	q
R	82	786	818	850	882	914	946	978	1010	114	r
S	83	787	819	851	883	915	947	979	1011	115	s
T	84	788	820	852	884	916	948	980	1012	116	t
U	85	789	821	853	885	917	949	981	1013	117	u
V	86	790	822	854	886	918	950	982	1014	118	v
W	87	791	823	855	887	919	951	983	1015	119	w
X	88	792	824	856	888	920	952	984	1016	120	x
Y	89	793	825	857	889	921	953	985	1017	121	y
Z	90	794	826	858	890	922	954	986	1018	122	z
[	91	795	827	859	891	923	955	987	1019	123	{
\	92	796	828	860	892	924	956	988	1020	124	|
]	93	797	829	861	893	825	957	989	1021	125	}
^	94	798	830	862	894	926	958	990	1022	126	~
_	95	799	831	863	895	927	959	991	1023	127	RUBOUT (DEL)
DEC →		56	57	58	59	60	61	62	63		
ASCII →		8	9	:	;	<	=	>	?		
		High Order X & Y									

Fig. 1-11. Coordinate conversion chart, part 4 of 4. (Refer to part 1 for interpretation instructions.)

CHARACTERISTICS

Introduction

The characteristics are in two parts. The first part consists of an alphabetic listing. The alphabetic listing makes reference to the second part, which contains tabulated information.

The following conditions must be met before all characteristics can be considered valid:

The Terminal must have been adjusted at an ambient temperature between +20°C and +30°C.

It must be operating in an environment as specified under Environmental Specification.

Operation must be preceded by a warmup period of at least 20 minutes.

Specified power requirements must be met.

The specifications pertain principally to On Line operation as selected at the keyboard rocker switch, and should not be presumed applicable to Local operation. Refer to the Local Operation specification for qualifying information.

The following tables are included immediately after the alphabetic listing of characteristics:

The characteristics included in the alphabetic listing are as follows:

Accessories
Address
Alpha Mode
Arming
Carriage Return
Character Effect on Terminal
Character Matrix
Character Size
Character Transmission in Alpha Mode
Character Transmission in GIN Mode
Character Writing
Character Writing Suppression
Characters, Lower Case
Clock
Control Character
Control Character Sequence
Cursor, Alpha
Cursor, Crosshair
Data Transfer Rate
Display Measurement Unit
Display Size
Display Unit Specifications
Echoplex
Echoplex Suppression
Environmental Specifications
GIN Mode
Graph Mode
Graphic Address
Graph Mode Memory
Graph Mode Vector Drawing
Hard Copy Mode
Hold Status
Home Position
Interface Specification
Line, Alpha Mode
Line Feed
Line Length, Graphic
Local Operation
Margin, Horizontal
Minibus
Modes
Options, Strappable
Pagefull
Physical Characteristics
Point (Tekpoint)
Power Supply Specifications
Receive Rate
Resetting GIN to Alpha Mode
Resetting Graph to Alpha Mode
Resetting Home Position
Resetting Margin 1 to Margin ∅
Space
Status Bits
Strappable Options
Tekpoint
Thumbwheels
Time, Character Writing
Time, Vector Drawing
Transmission, Alpha Mode
Transmission, GIN Mode
Transmission Rate
Vector Drawing Time
Vector Dynamic Geometry Error
Vector Length Error
View Mode

Alphabetic Listing

Accessories. See Table 2-14.

Address. A display position with reference to a grid of 1024 X 1024 points with 0, 0 being at the bottom left. Point density is about 130 points per inch horizontal or vertical with Terminal adjusted as outlined in the adjustment procedure.

Alpha Mode. A Terminal writing mode in which characters are written on the display screen. See Character Effect on Terminal and Table 2-2 for details.

Arming. Certain functions at the Terminal require a control sequence whose first character "arms" the Terminal, permitting the next character to perform a function other than what it would do if the Terminal were not armed. ESC is normally used as the arming command. The execution commands are listed under "Character Effect on Terminal". In addition, accessory devices may use other execution commands as explained in the accessory device instruction manual.

Carriage Return. Return of writing beam to the left or center margin (depending on effective margin position). Occurs on receipt of CR or ESC FF. Also occurs on receipt of LF if strapped on TC-1. Occurs automatically when beam spaces past 1023 address in Alpha Mode. Also caused by initializing or pressing PAGE key or SHIFT RESET keys. The CR character also causes a line feed to occur if the CR EFFECT option on TC-1 is in the CR→LF position. (The CR EFFECT option is not included in all instruments.)

Character Effect On Terminal. The Terminal recognizes all characters contained in the ASCII code. During Alpha Mode, all alphanumeric and graphic characters except space and delete result in character writing and subsequent spacing. Space does not write but causes spacing; delete causes neither writing nor spacing. Control characters and control character sequences are decoded and perform specific functions as shown in Table 2-1. Additional use of control characters or control character sequences may be made by accessory devices connected through circuit cards to the Terminal minibus. Control characters or control character sequences are recognized during Graph or GIN Mode; all other data received in Graph Mode is accepted as a vector address as explained in Graph Mode.

Character Matrix. A seven-by-nine dot pattern which creates characters by writing specific combinations of the dots. Dot position is determined by modifying the X or Y position of the deflection beam. The matrix stops long enough in each position to turn the beam on to store a dot during character writing, or to display a non-storing dot during Alpha Mode cursor writing. The bottom-left dot in the matrix is determined by the X and Y register contents (address). However, the X and Y deviation from this point is independent of the register address. The matrix is shifted down to write g, j, p, q, and y.

Character Size. Limits determined by character matrix, which is approximately .087 inch wide by 0.106 inch high.

Character Transmission in Alpha Mode. Depending upon the operation selected, the code for ASCII or TTY characters can be transmitted from the keyboard in response to a key, in response to a SHIFT and key combination, or in response to a CTRL SHIFT and key combination. RUBOUT sends the code for DEL. Bit 8 is sent as strapped at the keyboard (normally high), or as determined by the data communication interface in use. The minibus can accept any eight-bit combination from accessory units and transmit them to the computer.

Character Transmission in GIN Mode. A sequence of characters is transmitted to the computer in response to a control character sequence from the computer. See GIN Mode for details.

Character Writing. The Terminal has writing capability for all ASCII written characters. Since TTY is a subset of ASCII, TTY writing capability is included. Character writing time is approximately 1.0 ms.

Character Writing Suppression. The character generator is suppressed in GIN and Graph modes. The Alpha cursor, as well as alphanumeric characters, are prevented from being written. The character generator becomes fully enabled when the Terminal is switched from Graph to Alpha Mode. It also becomes fully enabled when GIN Mode is ended by an ESC FF or CR command from the computer, or by a PAGE or SHIFT RESET command from the keyboard. However, when GIN Mode is ended by transmitting the address of the Alpha cursor or the crosshair intersect address, the character generator will not become fully enabled unless the CR is sent as a part of the address transmission, *AND IS ECHOED BACK* by the computer. If CR is not echoed back, the Terminal will be unable to write in Alpha Mode (even though the Alpha cursor appears) until one of the following is received by the Terminal: BEL, BS, CR, ESC ETB, ESC FF, HT, LF, US, VT from the computer, or PAGE, SHIFT RESET, LOCAL, or MAKE COPY from the keyboard.

Characters, Lower Case. Lower case characters are accepted and written during Alpha Mode. Lower case letters cannot be transmitted from the keyboard while the TTY LOCK key is depressed.

Clock. The Terminal operates on an internal 4.9 MHz clock. This and a 614 kHz derivation are available on the minibus.

Control Character. See Character Effect on Terminal.

Control Character Sequence. See Character Effect on Terminal.

Cursor, Alpha. Flickering, non-storing seven-by-nine dot matrix which indicates position of writing beam. Occurs in Alpha Mode, during View condition. Position of lower-left corner of matrix is sent to computer in response to receipt of an ESC ENQ command sequence.

Cursor, Crosshair. GIN Mode non-storing cursor occurring in response to an ESC SUB command sequence. Cursor is caused by cycling of the X and Y registers through each point, pausing at each point long enough to write the point with an intensity insufficient for storing it. The intersect point can be moved to any point within 4-1023 X and 0-779 Y by using the keyboard X and Y thumbwheels. The address of the intersect point is sent to the computer in response to an ESC ENQ from the computer or in response to entering a keyboard character. See GIN Mode for explanation of transmission.

Data Transfer Rate. Interface dependent; limited to approximately 10,000 words per minute (average of six characters per word).

Display Measurement Unit. Point. Equivalent to one increment of X or Y position register. Approximately 130 points per inch and .0077 inch between centers of horizontally or vertically adjacent points. 1024 X points addressable and viewable; 1024 Y points addressable, 780 Y points viewable. (Terminal adjusted as outlined in adjustment procedure.)

Display Size. 8 inches horizontal by 6 inches vertical with its center within 0.25 inch of CRT faceplate center.

Display Unit Specifications. Refer to Table 2-9.

Echoplex. Consists of executing data at the Terminal as the data is being sent to the computer. Can be caused by placing an $\overline{\text{ECHO}}$ command on the minibus, usually from the interface unit.

Echoplex Suppression. Over-rides the $\overline{\text{ECHO}}$ signal from the interface unit, inhibiting echoplex operation. Occurs automatically when the Terminal is in GIN Mode, permitting the coded position data to be sent to the computer without being written by the Terminal, despite condition of the $\overline{\text{ECHO}}$ signal. See Table 2-6 for additional details.

Environmental Specifications. See Table 2-12.

GIN Mode. An interactive graphic mode which permits the Terminal to send one of the following to the computer: Terminal status and the position of the bottom-left corner of the Alpha cursor; or the Terminal status and the Graph Mode beam position; or the position of the GIN Mode crosshair intersect point. The crosshair intersect point is controlled by the thumbwheels at the right on the keyboard. Note that moving the horizontal thumbwheel to either limit may remove the vertical line from the display and disable the vertical thumbwheel. Similarly, moving the vertical thumbwheel to the lower limit may remove the horizontal line from the display and disable the horizontal thumbwheel. The Terminal status and Alpha cursor position is sent if ESC ENQ is received while the Alpha cursor is being displayed. Terminal status and Graph Mode beam position are sent if ESC ENQ is received while in Graph Mode. Receipt of ESC SUB causes the crosshair cursor to be displayed. Its intersect point is then sent in response to ESC ENQ from the computer, or in response to the operator entering a keyboard character.

A delay of at least 20 ms must occur between ESC SUB and ESC ENQ. The 20 ms delay can be ignored under several circumstances, as follows: (1) Whenever operating slower than 1000 baud; (2) Whenever only the Y address is required (X will always be sent, but may not be valid if the 20 ms delay is not used); and (3) If the Terminal is addressed to 0Y before sending the Terminal an ESC SUB. Addressing can be done by sending GS 40_8 140_8 and any Low X byte. (Actually, any Y value less than the crosshair intersect point can be used. Therefore, low Y byte 140_8 can be omitted unless the crosshair intersect point is located lower than the 16Y coordinate.) It should be noted that if the third option is used, the Terminal graphic memory circuit is loaded with the address. This can be used to advantage in repetitive requests for the crosshair posi-

tion; once loaded with a 0Y address, the Terminal need only be given a GS and a Low X byte to move the beam to 0Y. See Table 2-6 for GIN Mode details.

Graph Mode. A graphic display mode which occurs opon receipt of GS. It permits the Terminal to accept data as addresses. Movement to the address can either be dark or can result in drawing a vector. See Tables 2-3, 2-4, and 2-5.

Graphic Address. A combination of X and Y register values which indicates a position on the display (X 0-1023, Y 0-779) or off the display (Y 780-1023). Address of bottom-left corner of display is 0X, 0Y; address of top-right corner of display is 1023X, 779Y. See Tables 2-4 and 2-5 for information about sending an address to the Terminal.

Graph Mode Memory. The ability of the Terminal to remember the first three bytes of the last graphic address when switched out of Graph Mode. The Terminal requires receipt of only the low X byte to return to its last Graph Mode address when switched back to Graph Mode.

Graph Mode Vector Drawing. See Table 2-4.

Hard Copy Mode. Permits copying of the Terminal Display by a Hard Copy Unit. Mode is caused by $\overline{\text{READ}}$ from a Hard Copy Unit. $\overline{\text{TBUSY}}$ holds the Terminal busy during Hard Copy Mode. See Table 2-8.

Hold Status. A reduced intensity condition for the display unit. It occurs if the Terminal is inactive for approximately 90 seconds. The Terminal returns to View status as soon as data is received or a keyboard character is entered. Stored data may be retained in Hold status for up to one hour without damage to the screen.

Home Position. Top left corner of display unit in Alpha Mode, commanded by 0X, 767Y. Beam moves to that position upon initialization, and upon receiving ESC FF. It is also arrived at by entering PAGE or SHIFT RESET at the keyboard.

Interface Specification. See documentation pertaining to specific interface unit.

Line, Alpha Mode. Consists of 74 character spaces; lines are 22 points apart (approximately 0.17 inch) between identical reference points. 35 lines comprise the total display.

Line Feed. Moves writing beam down 22 points. This equals one line in Alpha Mode. Occurs upon receipt of LF. Occurs automatically when spacing past the end of a line. May also occur upon receipt of CR if the CR EFFECT option is at CR→LF.

Line Length, Graphic. Maximum line lengths within the quality display area are approximately 7.9 inches horizontal, 6 inches vertical, 9.9 inches diagonal. (Values given are within the display quality area with the Terminal adjusted as outlined in the adjustment procedure.)

Local Operation. Off-line operation used principally for operator training, formatting of data, and equipment maintenance. It is selected by the LOCAL/LINE switch at the keyboard, and isolates the Terminal from the computer. See Table 2-7 for details.

Margin, Horizontal. Margin Ø is located at 0X; Margin 1 is located at 512X. Margins alternate automatically when line-feeding past the 35th line. Carriage return resets the beam to selected margin. ESC FF resets the Terminal to Margin Ø. Terminal also resets to Margin Ø in response to PAGE key or SHIFT RESET key combination.

Minibus. Signals available at each of the board-edge connectors on the motherboard. See Dictionary of Line Titles and Wire List in the Circuits section for details.

Modes. Alpha (Alphanumeric), Graph (Graphic Display), GIN (Graphic Input), Hard Copy. See Specific mode descriptions for details.

Options, Strappable. See Table 2-13 for strappable options for the basic Terminal; see interface unit documentation for strap option information pertaining to interface units.

Pagefull. A condition occurring in Alpha Mode when line-feeding past the 35th line. It causes Margin 1 to occur (center of screen) if Margin Ø has been set, and vice-versa. Margin 1 can cause a terminal busy signal, if selected by option on TC-2.

Physical Characteristics. See Table 2-11.

Point (Tekpoint). The basic unit of measurements for Graph and GIN Modes. 1024X (0-1023) and 1024Y (0-1023) points addressable; 1024X and 780Y (0-779) viewable. Point spacing is approximately .0077 inch. (Approximately 130 points per inch.) (Terminal adjusted as outlined in the adjustment procedure.)

Power Supply Specifications. See Table 2-10.

Receive Rate. Capable of ⩾10,000 words per minute (average of six characters per word). Interface dependent.

Resetting GIN to Alpha Mode. GIN Mode is cancelled and Alpha Mode reset upon receipt of CR or ESC FF from the computer. Resetting with CR may leave the Terminal in Margin 1 status. It would be better to permit transmission of address and ignore it at the computer to insure that the Terminal returns to Margin Ø status. Resets to Alpha (without transmitting to computer) in response to entering PAGE or SHIFT RESET at the keyboard. Terminal also resets to Alpha Mode after completing GIN transmitting function. Refer to Table 2-6 for details.

Resetting Graph to Alpha Mode. Graph Mode is cancelled and Alpha Mode reset in response to US, CR, or ESC FF from the computer. It can also be reset by entering PAGE or SHIFT RESET at the keyboard.

Resetting Home Position. The Terminal display resets to home position (top-left of display) in response to ESC FF from the computer. It also resets to home position in response to line-feeding past line 35 if Margin 1 exists and the TC-1 option is set so that line feed causes carriage return. Home position also occurs when PAGE or SHIFT RESET is entered at the keyboard.

Resetting Margin 1 to Margin Ø. Margin 1 (horizontal center of display) resets to Margin Ø (left edge of display) in response to ESC FF from the computer, or in response to an LF (line feed) past the 35th line. Margin Ø also occurs in response to PAGE or SHIFT RESET entered at the keyboard.

Space. An Alpha Mode measurement made from a reference point in a character to the same reference point in a horizontally adjacent character. A space is equal to 14 Tekpoints, which equates to approximately 0.11 inch. There are 74 spaces per line.

Status Bits. Bits transmitted in GIN Mode to denote the status of the Terminal. They are transmitted as part of a response to an ESC ENQ received while in Alpha or Graph Mode, and consist of the following:

Bit 8 = 1, Bit 7 = Ø, Bit 6 = 1.

Bit 5 = Hard Copy Unit status; Ø is intended to mean that the Hard Copy Unit is in working order, ready to accept a hard copy request.

Bit 4 = Vector status indicator. A 1 indicates that the Terminal is set up to draw vectors.

Bit 3 = Graphic Mode indicator. A Ø indicates that a graphic mode exists. 1 indicates Alpha Mode.

Bit 2 = Margin indicator. 1 indicates that Margin 1 exists. Ø indicates Margin Ø. If the Margin bit is 1 (true), it indicates that the Alpha cursor is on the right half of the screen. If the transmitted X address is less than 512, it must be increased by 512 to indicate its position with respect to the left edge of the screen. Effectively, if the Margin bit is 1 (true), the most significant X bit (512 bit) must be considered to be true regardless of what value was transmitted by the terminal.

Bit 1 = Auxiliary device indicator. Ø indicates that some optional auxiliary unit is activated.

Strappable options. Optional operating features which can be selected by connectors within the Terminal. See Table 2-13.

Tekpoint. A unit of measurement associated with Tektronix Terminals. It consists of the distance between two adjacent points in the 1024 x 1024 grid provided by the X and Y registers. See Point.

Thumbwheels. Potentiometers located on the keyboard; used to position the crosshair cursor.

Time, Character Writing. Approximately 1.0 ms.

Time, Vector Drawing. Time required to draw a complete vector in a standard Terminal is approximately 2.6 ms.

Transmission, Alpha Mode. Data is transmitted as entered at the keyboard, or as placed on the minibus by other devices.

Transmission, GIN Mode. Data is transmitted as a series of bytes in response to an ESC ENQ from the computer, or in response to a keyboard character entered while the cross-hair cursor is displayed. Refer to Table 2-6 for details.

Transmission Rate. Interface dependent. See documentation pertaining to the specific interface unit. Also see Data Transfer Rate.

Vector Drawing Time. 2.6 ms or less.

Vector Dynamic Geometry Error. Deviation (due to vector generator circuitry) from mean straight line does not exceed 1.5% worst case (45° line).

Vector Length Error. Does not exceed 1% of actual vector length.

View Status. Normal intensity display. Occurs at all times except during copy making (Hard Copy Mode) and Hold status. Alpha Mode View status occurs upon keyboard entry or upon receipt of data, and remains for 60 to 120 seconds. It can be regained without affecting the display or causing transmission by pressing the SHIFT key. The Terminal remains in View status whenever in Graph or GIN Modes. The Terminal can remain in View status with a stored display for 15 minutes without permanent damage to the display screen.

TABLE 2-1

Control Character Effect on Terminal

Control Character	Keyboard Command	Effects
BEL	CONTROL G	A burst of 1200 hertz tone on the speaker. Makes Terminal go busy for approximately 200 ms. Sending a character or vector to the Terminal during the tone burst will terminate that burst.
BS	BACKSPACE or CTRL H	Backspaces one space. Backspacing to the left of the margin will cause wraparound.
CR	RETURN or CTRL M	Causes carriage return by clearing X register. Also causes line feed if the CR EFFECT option on TC-1 is at CR→LF. (The CR EFFECT option is not included in all instruments.) Clears GIN and Graph. (If the crosshair is cleared with CR, the resulting status of Y and Margin perform the Page Full function. With interfaces directly connected to the CPU, it is better to clear the cursor by sending ESC ENQ or ESC FF.)
ESC	ESC or CTRL SHIFT K	First character of a special multiple-character sequence. ESC activates LCE (B on the Minibus) which remains high until after the trailing edge of the next byte or activation of $\overline{\text{HOME}}$. Does not cause a response on $\overline{\text{TBUSY}}$.
ESC ENQ	ESC CTRL E	Causes Terminal status and/or Alpha cursor or Graph beam or crosshair cursor position to be sent to CPU. Useful for remote diagnostics, in addition to graphic uses. Local copy is not generated. See explanation under GIN Mode. Activates echoplex suppression. If the $\overline{\text{CSTROBE}}$(s) generated does not cause a $\overline{\text{CBUSY}}$ response, the Terminal will remain in GIN Mode. This occurs if ESC ENQ is entered while in LOCAL; can be cleared by PAGE or SHIFT RESET entry. Does not cause a response on $\overline{\text{TBUSY}}$.
ESC ETB	ESC CTRL W	$\overline{\text{MAKE COPY}}$ is asserted.
ESC FF	ESC CTRL L	Same as PAGE signal from keyboard. Erases screen. Resets X to 0. Resets Y to 767. Resets GIN, Echoplex Suppression, Margin, and Graph.
ESC SI	ESC CTRL O	If strap on TC-1 is set for AB+BC, selects the ASCII Character Set. Does not cause a response on $\overline{\text{TBUSY}}$.
ESC SO	ESC CTRL N	If strap on TC-1 is set for AB+BC, selects the Alternate Character Set. Does not cause a response on $\overline{\text{TBUSY}}$.
ESC SUB	ESC CTRL Z	Clears Graph. Starts crosshair cursor (which sets GIN). Activates Echoplex Suppression. (See explanation under ESC ENQ.) Does not cause a response on $\overline{\text{TBUSY}}$.
GS	CTRL SHIFT M	Sets Terminal to Graph Mode; sets for dark vector. Does not cause a response on $\overline{\text{TBUSY}}$.
HT	TAB or CTRL I	Spaces one space to right.
LF	LF or CTRL J	Y moves down one line (counts down by 22). If Y counts through 0, margin switches between 0 and 1, and Y counts down to 767. Strap on TC-1 can be set so that LF also causes carriage return.
US	CTRL SHIFT O	Clears Terminal from Graphic Display Mode.
VT	CTRL K	Inverse line feed. Y counts up by 22. If Y exceeds 767 in Alpha Mode, Y will count back down to 767.

TABLE 2-2

Alpha Mode Specification

Writing Area	8 inches horizontal by 6 inches vertical.
Character Writing Position	Indicated by pulsating cursor (7 x 9 dot matrix), approximately .087 inch wide by 0.106 inch high (11 x 14 points).
Character Recognition	Complete ASCII code is recognized.
Character Writing	All ASCII writing characters are written upon receipt.
Character Size	Size of largest character is approximately .087 x 0.106 inch (11 x 14 points) written within limits of 7 x 9 dot matrix.
Character Writing Time	Approximately 1.0 ms, providing at least 1000 characters per second.
Characters Per Line	74
Space	14 Tekpoints (equal to approximately 0.11 inch) between corresponding points in adjacent characters.
Number of Lines	35 lines.
Line Feed Spacing	22 Tekpoints (approximately 0.17 inch) between corresponding points on adjacent lines.
Carriage Return/Line Feed	Automatically occurs after character is written at end of line (74th character). Strap option can be set to cause carriage return to occur in response to programmed line feed.
Margin	Margin Ø (left edge) and Margin 1 (horizontal center) alternately occur when line-feeding past the bottom (35th) line.
Rubout	Does not print or space.
Home	Top-left corner of display (0X, 767Y).
Pagefull	Occurs when line-feeding past 35th line with Margin 0 set.
Alpha Mode set by	Initialization; PAGE or SHIFT RESET at keyboard; receipt of ESC FF or CR.
Writing Rate	⩾10,000 words per minute (average of 6 characters per word).
Cursor	Non-storing, pulsating 7 x 9 dot matrix.
Hold	Reduced intensity status which occurs in Alpha Mode only; occurs after approximately 90 seconds of inactivity. Stored display can be retained for up to one hour in Hold status without damage to the display screen.
View	Normal viewing status. Stored data can be displayed in View status for up to 15 minutes without damage to display screen.
Character Type	
Transmitting	Full ASCII code can be transmitted. TTY LOCK limits transmission to TTY code.
Receiving	Full ASCII code can be written, regardless of position of TTY LOCK key.

TABLE 2-3

Graph Mode Specification

Mode Function	Display graphic information.
Mode Commanded By	GS.
Mode Ended By	US, CR, ESC FF, ESC SUB, or keyboard entry of PAGE or SHIFT RESET.
Basic Unit of Measurement	Point (Tekpoint).
Address Capability	1024X by 1024Y points.
Display Capability	1024X by 780Y points.
Display Address Orientation	0, 0 at bottom-left of display; 1023X, 779Y at top-right.
Display Area	7.88 inches horizontal by 6 inches vertical.
Vector Length Error	Does not exceed 1% of actual vector length.
Vector Writing Time	2.6 ms in standard Terminal.
Vector Dynamic Geometry Error	Deviation from prescribed path does not exceed 1.5% of total line length. This is exclusive of the 0.5% Line Straightness specification of the display circuits.
Display Scale Factor	Approximately .0077 inch, point center to point center (approximately 130 points per inch).
Dark Vectors	First vector to follow GS is unwritten. GS can be repeated at any time. Second vector following GS, and all subsequent vectors, are written.
Viewing Time	Indefinite; Hold status is inhibited. (Terminal should be returned to Alpha Mode when not in use. Stored display can be displayed in View status for up to 15 minutes without damage to the display screen.)
Vector Drawing Commands	See Tables 2-4 and 2-5.
Margin	Margin 1 is disabled.
Graph Mode Memory	First three bytes of last Graph Mode address are remembered when the Terminal is switched out of Graph Mode. Terminal requires only the Low X byte to return to its last graphic address when switched back to Graph Mode.

TABLE 2-4

Graph Mode Vector Drawing

(1)	GS Places the Terminal in Graph (Vector) Mode.	
(2)	The Terminal can be addressed to any position within 0-1023X and 0-1023Y as follows:	
	(A)	Convert Y coordinate to ten binary digits; convert X coordinate to ten binary digits.
	(B)	Form a Hi Y byte by affixing 01 (as bits 7 and 6) to the 5 MSB of the ten digits of the Y coordinate.
	(C)	Form a Lo Y byte by affixing 11 (as bits 7 and 6) to the 5 LSB of the ten digits of the Y coordinate.
	(D)	Form a Hi X byte by affixing 01 (as bits 7 and 6) to the 5 MSB of the ten digits of the X coordinate.
	(E)	Form a Lo X byte by affixing 10 (as bits 7 and 6) to the 5 LSB of the ten digits of the X coordinate.
	(F)	Send the four bytes as formed in (B) through (E).
(3)	The Lo X byte causes the beam to move to the new position. The first movement after a GS is unwritten (dark vector). Subsequent movement in response to a Lo X byte is written to form a vector. GS can be sent at any time to cause the next vector to be dark. (780Y-1023Y is outside the viewing area of the horizontally oriented display.)	
(4)	Address transmission can consist of all four bytes or can be shortened to 3, 2, or 1 byte(s). Omitted bytes are assumed to be correct as held in the Terminal. Table 2-5 specifies the minimum byte transmission that is required under all addressing situations.	
(5)	Hi Y, Lo Y, and Hi X bytes of the last address received are "remembered" by the Terminal if switched to Alpha or GIN Mode. The Terminal requires receipt of only the Low X command to return to its last address after being switched back to Graph Mode.	

TABLE 2-4 (cont)

(6)	Hold status is inhibited during Graph Mode. A stored display should not be retained in Graph Mode for more than 15 minutes.
(7)	Graph Mode is ended by US, CR or ESC FF, which reset the Terminal to Alpha Mode. Graph Mode can also be ended by ESC SUB, which switches the Terminal to GIN Mode. PAGE and SHIFT RESET from the keyboard also end Graph Mode, resetting Alpha Mode.
(8)	$\overline{\text{TBUSY}}$ does not occur in response to Hi Y, Lo Y, Hi X.

TABLE 2-5

Bytes Required for Graphic Addressing

Bytes Which Change				Byte Transmission Required			
Hi Y	Lo Y	Hi X	Lo X	Hi Y	Lo Y	Hi X	Lo X
			#				#
		#			#	#	#
	#				#		#
#				#			#
		#	#		#	#	#
	#		#		#		#
#			#	#			#
	#	#			#	#	#
#		#		#	#	#	#
#	#			#	#		#
	#	#	#		#	#	#
#		#	#	#	#	#	#
#	#		#	#	#		#
#	#	#		#	#	#	#
#	#	#	#	#	#	#	#
Sending initial address				#	#	#	#
Returning to remembered address							#

Ⓐ

TABLE 2-6

GIN Mode Specifications

Functions	
Transmit Terminal Status and Alpha Cursor Position	With Alpha cursor displayed, the Terminal status, address of bottom-left corner of Alpha cursor, CR[1] and EOT[1] are transmitted to the computer in response to ESC ENQ from the computer. The Terminal automatically resets to full Alpha Mode upon completion of sending the following bytes if CR is echoed by the computer. Otherwise, the Terminal must be reset as explained under Echoplex Suppression. Note that if CR is echoed, it resets the cursor to the effective margin position.
Transmit Terminal Status and Graph Mode Beam Position	If ESC ENQ is received while in Graph Mode, bytes 1 through 7 will be sent as explained above. Echoing of the bytes by the computer is not recommended because echoing of bytes 1 through 5 will affect the content of the Y memory latch, and echoing of CR will reset the Terminal to Alpha Mode.
Display Crosshair Cursor	ESC SUB from the computer turns the crosshair cursor on. (ESC SUB should not be entered at the keyboard.) This is a preparatory state for transmitting the address of the crosshair intersect point. The Terminal can be reset to Alpha Mode by ESC FF without causing it to transmit the crosshair intersect address. The Terminal can also be reset to Alpha Mode by a PAGE or SHIFT RESET command entered at the keyboard, without transmitting the crosshair intersect address.
Transmit Crosshair Intersect Address	
In Response to ESC ENQ	With crosshair cursor displayed, ESC ENQ from the computer causes transmission of bytes 2 through 7 as previously listed. The Terminal automatically returns to full Alpha Mode upon completion of transmission if CR is echoed by the computer. Otherwise, the Terminal must be reset as explained under Echoplex Suppression. A 20 ms delay must exist between ESC SUB and ESC ENQ. The 20 ms delay can be ignored under several circumstances, as follows: (1) Whenever operating slower than 100 baud; (2) Whenever only the Y address is required. (X will always be sent, but may not be valid if the 20 ms delay is not used); and (3) If the Terminal is addressed to 0Y before sending the Terminal an ESC SUB.

Bytes transmitted (Transmit Terminal Status and Alpha Cursor Position):

Byte	Item	Bit 7	Bit 6	Bits 5–1
1	Terminal Status	0	1	Status Bits
2[2]	High bits of X address	0	1	5 MSB X
3	Low bits of X address	0	1	5 LSB X
4	High bits of Y address	0	1	5 MSB Y
5	Low bits of Y address	0	1	5 LSB Y
6	CR[1]	0	0	01101
7	EOT[1]	0	0	00100

[1]CR and EOT are optional, being dependent on straps on TC-2. EOT, or CR and EOT may be omitted. EOT cannot be sent without sending CR.

[2]If the Margin bit of the Terminal Status Byte is 1 (true), the most significant X bit (512 bit) must be considered to be true, regardless of the value transmitted to the computer.

TABLE 2-6 (cont)

Transmit Crosshair Intersect Address (cont)	
In Response to Keyboard Character Entry	With crosshair cursor displayed, a keyboard character entry causes the Terminal to transmit the keyboard character, and then to transmit bytes 2 through 7 as previously listed. The Terminal automatically returns to full Alpha Mode upon completion of transmission if CR is echoed by the computer. Otherwise, the Terminal must be reset as explained under Echoplex Suppression.
Address	
Basic Unit of Measurement	Point (Tekpoint).
Alpha Cursor	
Limits	0 to 1023X, 0 to 767Y, inclusive.
Transmission Accuracy	Actual address of lower left corner is transmitted. However, if Margin 1 exists (as indicated by bit 2 of the status byte being true) the most significant X bit (512X) must be considered to be true, regardless of how it was transmitted by the Terminal.
Crosshair Cursor	
Limits	4 to 1023X, 0 to 779Y, inclusive.
Controlled by	Horizontal and vertical thumbwheels at right on keyboard panel.
Transmission Accuracy	Within ±1 point of actual position of crosshair cursor intersect point.
Status Bits	Bit 8 = 1, Bit 7 = Ø, Bit 6 = 1.
	Bit 5 = Hard Copy Unit status; Ø is intended to mean that it is in working order, ready to accept a hard copy request.
	Bit 4 = Vector status indicator. 1 indicates that the Terminal is set to draw vectors.
	Bit 3 = Graph Mode indicator. Ø indicates that a graphic mode exists; 1 indicates Alpha Mode.
	Bit 2 = Margin indicator. 1 indicates that Margin 1 exists; Ø indicates Margin Ø. See note 2.
	Bit 1 = Auxiliary device indicator. Ø indicates that some optional auxiliary device is activated.
Echoplex Suppression	Over-rides local echoing and disables character generator during GIN Mode. The receiving circuits automatically become enabled upon completion of transmission if CR is echoed by the computer. If CR is not echoed, the Terminal must be reset by BEL, BS, CR, ESC ETB, ESC FF, HT, LF, US, or VT from the computer, or by entering PAGE, RESET, LOCAL, or MAKE COPY at the keyboard. Resetting is not required in Graph Mode.
Byte Format	8 bits. In Terminals equipped with a Data Communication Interface 021-0065-00, bit 8 is determined by a strap on the keyboard which is factory-wired to 1, but may be changed to zero. In other interface units, bit 8 may be controlled by the keyboard strap or by the interface unit.

[2] If the Margin bit of the Terminal Status Byte is 1 (true), the most significant X bit (512 bit) must be considered to be true, regardless of the value transmitted to the computer.

TABLE 2-7

Local Operation Specification

General	The Terminal is isolated from the computer.
Alpha Mode	Terminal accepts keyboard data as though it were coming from a computer, writing alphanumeric characters and executing control characters.
GIN Mode	Crosshair cursor can be obtained by entering a sequence consisting of ESC and CTRL Z. The cursor is under full control of the thumbwheels. The keyboard is locked out; the cursor will not disappear in response to striking a keyboard key as it does when on-line. The Terminal can be reset to Alpha Mode by entering PAGE or SHIFT RESET at the keyboard.
Graph Mode	Can be obtained by entering CTRL SHIFT M at the keyboard. Terminal will then write vectors in response to keyboard entries of graphic addresses as explained in Tables 2-3, 2-4, and 2-5. Obviously, the addresses must be converted to alphanumerics before knowing which keys send which address bytes. Dark vectors will follow any CTRL SHIFT M entries. The Terminal retains the ability to execute control characters.

TABLE 2-8

Hard Copy Mode Specification

Function	Display is scanned by signals from the Hard Copy Unit, providing readout information to the Hard Copy Unit.
Initiated By	$\overline{\text{READ}}$ signal from Hard Copy Unit. ($\overline{\text{READ}}$ occurs in response to a Make Copy command from the keyboard, a copy command from the Hard Copy Unit, or an ESC ETB sequence from the computer.)
GIN Cursor	Inhibited.
Alpha Cursor	Inhibited.
Hold Mode	Inhibited.
Display Unit	Under control of Hard Copy Unit.
Terminal Busy	Asserted.
GIN Mode	If commanded during Hard Copy Mode, the GIN transmission is delayed until copying is completed.

TABLE 2-9

Display Unit Specifications

Characteristics	Performance Requirements	Supplemental Information
Display Quality Area	8 inches horizontal by 6 inches vertical, whose center is within 0.25 inch of the CRT faceplate center.	
Deflection Factors		
Center of Screen		Zero volts.
Edge of Screen		+5.0 volts left or down, –5.0 volts right or up.
Usable Storage Time		Up to 15 minutes in View status or up to one hour in Hold status without permanent damage to the storage screen. If a residual image is retained after a long viewing period, the screen may sometimes be returned to normal condition by repeated erasures.
Line Straightness	Within 0.5% deviation from mean straight line (inside the specified display area).	This is a function of the display circuitry and does not include the 1.5% dynamic geometry specification of the vector generator circuitry.
Geometry		
Orthogonality		$\leqslant 1°$.
Parallelism	Within ±2%.	Condition for Test; Draw a rectangle on edge of specified area. Difference between lengths of vertical lines should be within 2% of length of horizontal line. Difference between lengths of horizontal lines should be within 2% of length of a vertical line.

TABLE 2-10

Power Supply Specifications

Characteristics	Performance Requirements		Supplemental Information
Line Voltage Ranges	110 V AC	220 V AC	Wiring connections are listed on the inside surface of the pedestal's front cover.
Low	110 V ±10%	100 V ±10%	
Medium	115 V ±10%	220 V ±10% 230 V ±10%	
High	120 V ±10%	240 V ±10%	
Power Consumption			192 watts maximum.
Line Frequency Range	48 to 440 Hz.		
Fuses	2 A slo-blo for 110 V operation. 1.25 A slo-blo for 220 V operation.		

TABLE 2-11

Physical Characteristics

Finish	Metal and plastic painted cabinet.
Weight	Approximately 90 lbs. (shipping weight approximately 107 lbs.).
Dimensions, Overall	See Fig. 2-1.
Height	About 41.5 inches.
Width	About 19.25 inches.
Length	About 29 inches.

TABLE 2-12

Environmental Specifications

Temperature	
Non-operating	–40° C to +65° C.
Operating	+10° C to +40° C.
Altitude	
Non-operating	To 50,000 feet.
Operating	To 15,000 feet.
Vibration (Non-operating)	Complete terminal: Not specified. Display Only: 10-40-10 c/s @ .010 inch total displacement. Pedestal Only: 10-40-10 c/s @ .010 inch total displacement.
Shock (Non-operating)	To 20 Gs, 1/2 sine, 11 ms duration.
Transportation	Meets National Safe Transit Committee type of test when packaged as shipped by factory.

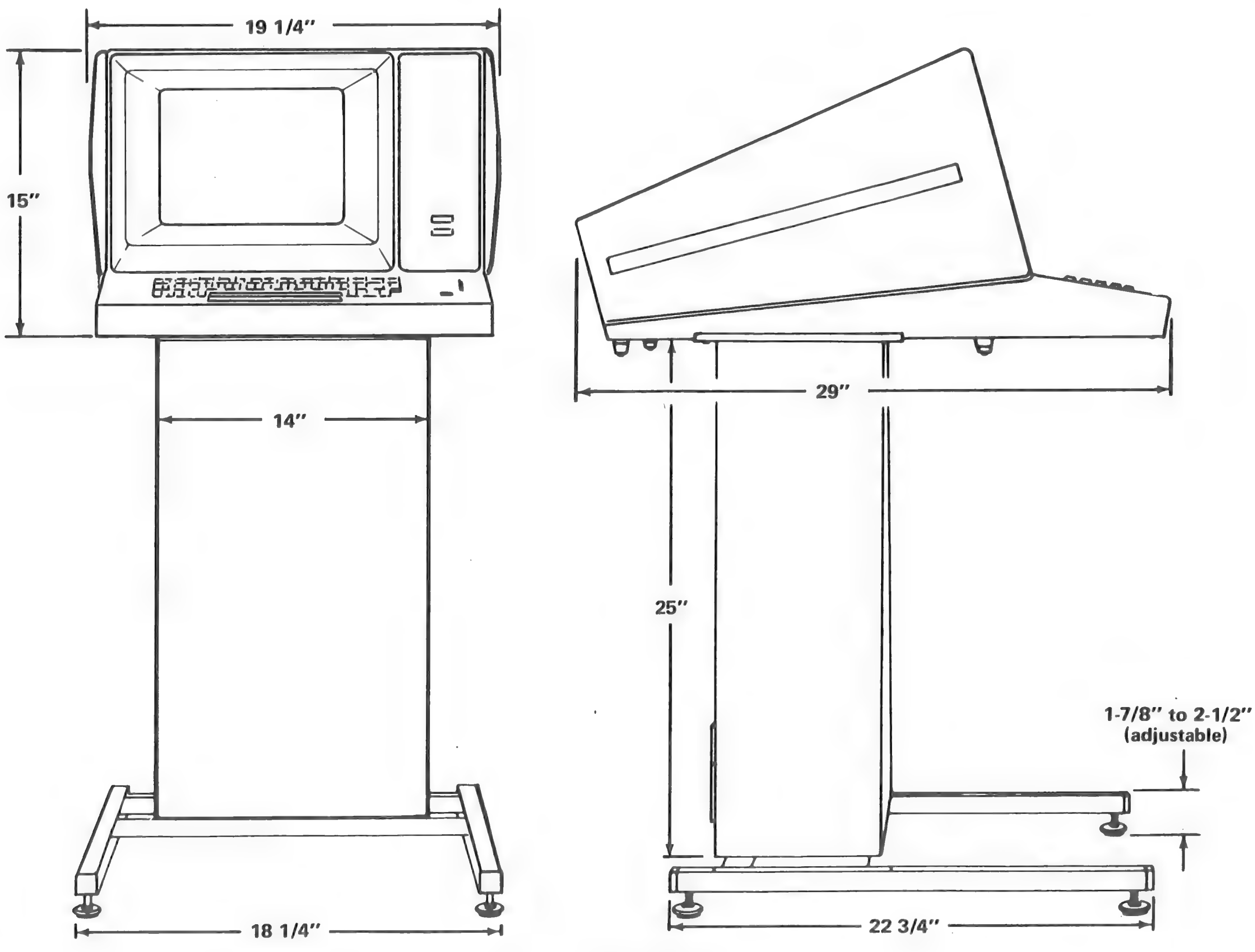


Fig. 2-1. Overall Dimensions.

TABLE 2-13
Strappable Options of Basic Terminal (See Fig. 2-2)

Feature	Location	Choice	Effect
LF Effect	TC-1, Top row		LF causes Line Feed only; LF→CR causes Line Feed and Carriage Return
CR Effect (not included in all instruments)	TC-1, Top row		CR causes Carriage Return only; CR→LF causes Carriage Return and Line Feed
ROM Select	TC-1, 2nd row		AB+BC permits program or switch selection of alternate character set; AB inhibits selection of alternate character set
Graphic Input Terminators	TC-2, Top row		CR & EOT transmits CR & EOT in GIN Mode; CR transmits CR in GIN Mode; NONE transmits neither CR nor EOT in GIN Mode
PF Break	TC-2, 4th row		OUT prevents a page full from causing a busy signal; IN permits a page full to generate a Terminal busy signal (TBUSY)
Display Multiplexer Bypass Cable	Bottom-left on motherboard; second plug from bottom (P33)	(1) Connect to J33 on motherboard; (2) Connect to Display Multiplexer card (optional card)	(1) Terminal Control circuits directly control the display (2) Terminal Control circuits control the display at the discretion of an optional Display Multiplexer card

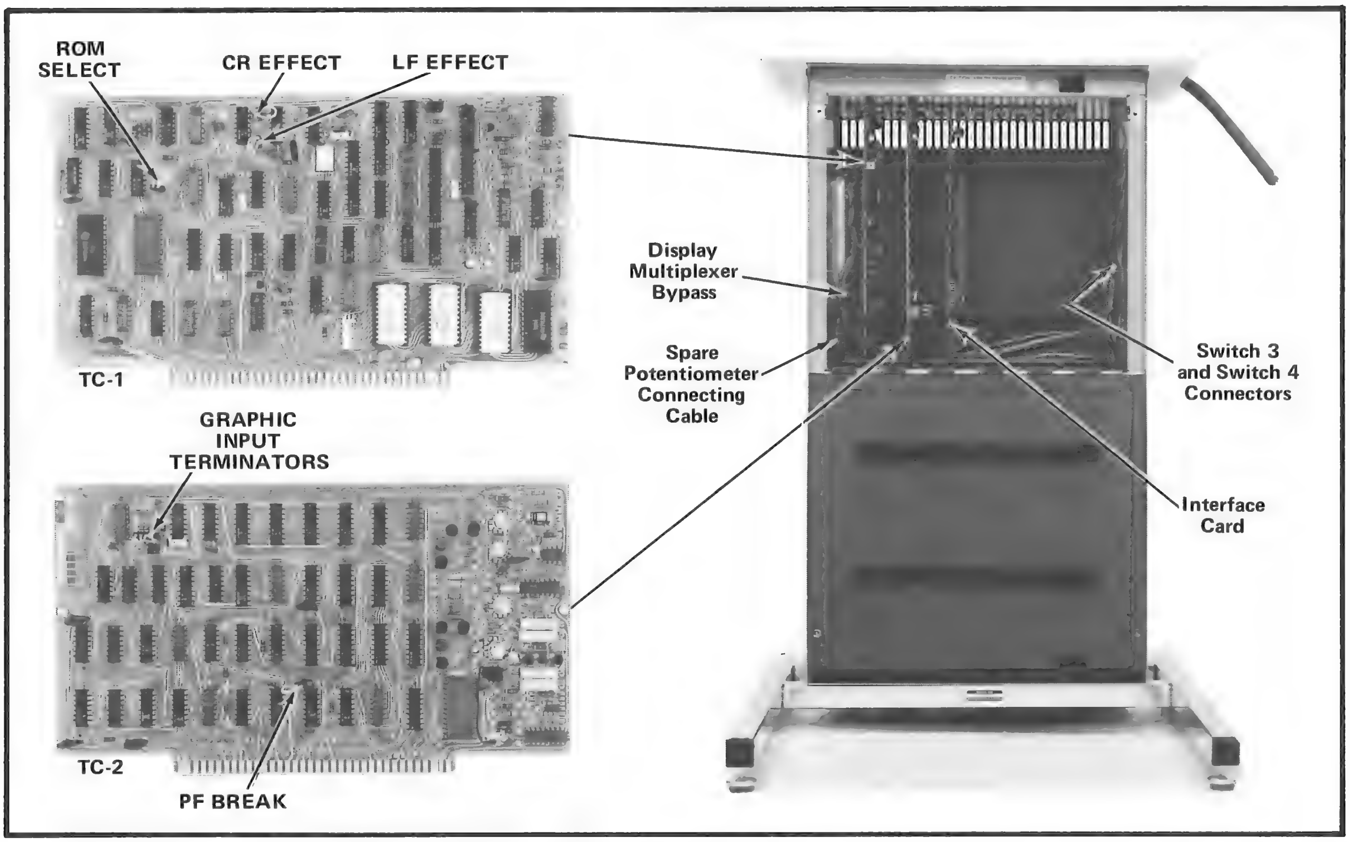


Fig. 2-2. Location of Strappable options. Additional Strappable Option information is given in Table 2-13. Locations of TC-1, TC-2, and the Interface are interchangeable.

TABLE 2-13 (cont)

Feature	Location	Choice	Effect
Spare Potentiometer Connection	Bottom-left on motherboard; bottom plug (P34)	(1) Connect to J34 on motherboard; (2) Connect to optional circuitry	(1) Dead-ended (2) Provides connection to wiper of spare 50 kΩ potentiometer (bottom surface of Display Unit), which is connected between +5 V and +15 V.
Switch 3 and Switch 4 Connections	On top-right wall within pedestal	(1) Disconnected; (2) Connected to optional circuitry	(1) No effect (2) Provides ground connections via Switch 3 and Switch 4 on keyboard

TABLE 2-14

Accessories for the Terminal

Item	Part No.
STANDARD ACCESSORIES	
Data Communication Interface	021-0065-00
4012 User's Manual	070-1460-00
OPTIONAL ACCESSORIES	
4012 Service Manual	070-1461-00
Logic Extender Card	067-0653-00
Audio Recorder Interface	018-0066-01
Motherboard Extender	018-0069-00
Display Multiplexer	018-0067-00
Copy Holder	016-0291-00
72-Pin Extender Card	670-1739-00
Auxiliary Card (empty thru-hole plated card for circuit development)	018-0065-00
Auxiliary Card (similar to 018-0065-00, but contains ground and VCC bus lines; ideal for use where large quantities of IC's are involved.)	018-0068-00
Optional Data Communication Interface	021-0074-00
TTY Port Interface (part number varies with type of installation)	021-xxxx-xx
Access Cover, Optional (for dual interface installation)	200-1288-01

MAINTENANCE

INTRODUCTION

Beyond the need for occasional cleaning of the face of the display and other outer surfaces of the Terminal, there is virtually no need for routine servicing of the Terminal. It has no lubrication points, no air filters, and (with the exception of the CRT) no vacuum tubes. The solid-state components provide stable operation, with little need for routine adjustment.

However, if a routine schedule and procedure is desired, a one-year interval and the following sequence is recommended. The disassembly and assembly instructions contained in this section should be referred to as necessary.

Desk-Mounting the Display Unit

The display unit and pedestal are connected only by a cable during shipment. Desk-mounting consists of simply setting the display unit on a desk or other surface. See Fig. 3-1(A). The pedestal can be placed as far as four feet away from the display unit. The air vents on the bottom and back should be kept free of obstructions. Note that if the base (leg assembly) is removed from the pedestal, the feet should be unscrewed from the base and inserted into the bottom of the pedestal to permit air flow into the bottom vents. However, make certain that the base is re-installed before the display unit is again placed on the pedestal.

If the display unit has been mounted on the pedestal, desk-mounting consists of reversing the pedestal-mounting procedure and observing the instructions which have just been outlined.

Pedestal-Mounting the Display Unit

Mounting the display unit on the pedestal is best accomplished by two people. It includes the following steps; refer to Fig. 3-1(B) as necessary.

1. If the Terminal has previously been used in a desk-top configuration, the base (leg assembly) may have been removed from the pedestal and the feet installed directly into the bottom of the pedestal. In that event, put the feet back on the base, and fasten the base to the bottom of the pedestal.

2. Lift the display unit over the pedestal as shown in the accompanying illustration.

3. Feed the cable down into the front of the storage bin as far as possible, while lowering the display unit into place. Then double the cable back and forth in the storage bin as lowering of the display unit continues.

4. There is a retaining strip on the bottom of the display unit. Slide it over the back edge of the pedestal top. Install four machine screws up through the pedestal top to fasten the display unit in place.

5. Adjust the four feet to a convenient position, and fasten the lock nuts.

Servicing Procedure

(1) Disconnect the line cord from the power source.

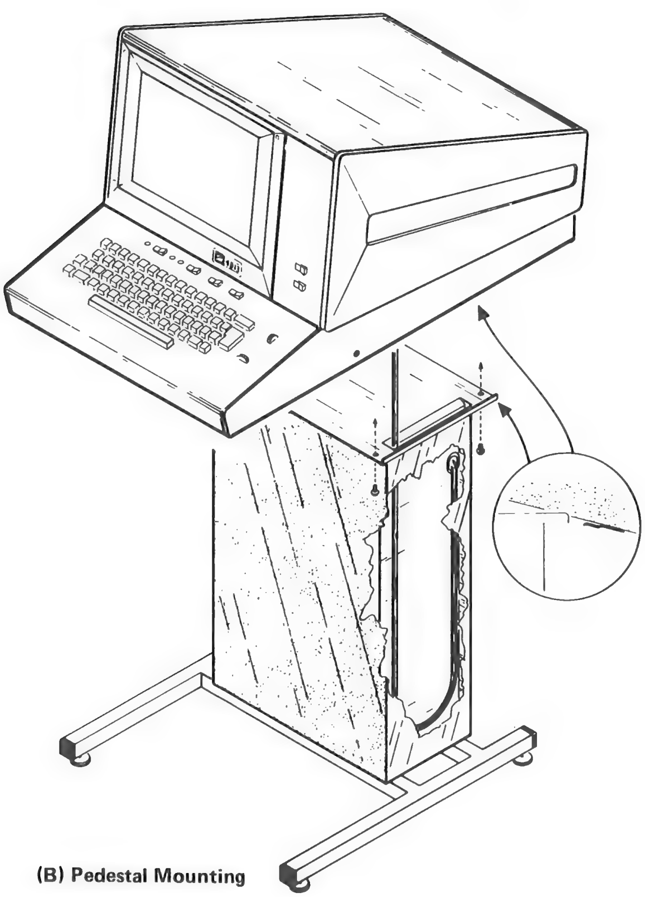
(2) Unbolt the display unit from the pedestal and set them adjacent to each other on a work surface.

(3) Remove the top from the display unit and the front from the pedestal.

(4) Using a vacuum cleaner, remove dust accumulation from within both units. Use a soft-bristled brush to loosen dust which won't otherwise vacuum out. A soft cloth and a mild soap and water solution can be used to remove any really stubborn dirt.

(5) Inspect the interior of both units for broken leads, loose connections, heat damaged components, etc. Correct as necessary. Investigate the cause of any heat-damaged components.

(A) Desk Mounting



(B) Pedestal Mounting

Fig. 3-1. Mounting The Display Unit.

(6) Remove the graticule mask and the filter from the front of the display screen. Then wash the face of the CRT and the back surface of the filter, using a soft cloth and a mild soap and water solution. Then replace the filter and graticule mask. *THIS STEP SHOULD NOT NORMALLY BE NECESSARY, SINCE A NEOPRENE MOUNTING RING SEALS THE SPACE BETWEEN THE FACE OF THE CRT AND THE FILTER. IT IS RECOMMENDED ONLY IF DIRT IS VISIBLE BETWEEN THE TWO SURFACES, OR IF THE DISPLAY APPEARS EXCESSIVELY DIM AND DIRT ACCUMULATION IS SUSPECTED.*

(7) Perform the check-out procedure found in this manual. Perform the adjustment procedure if the check-out procedure indicates that it is necessary.

(8) Put the covers back on the display unit and on the pedestal. Install the display unit on the pedestal, if desired.

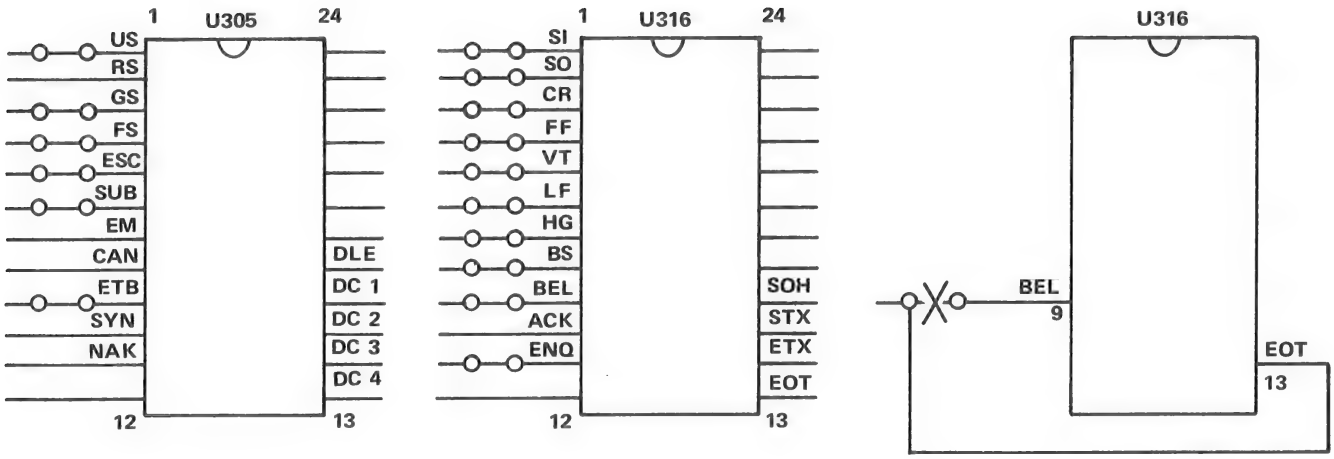
(9) Clean the outside of the units, using a soft cloth and a mild soap and water solution. Use particular care in cleaning the external surface of the display filter.

Soldered Options

In addition to strappable options, there are some options which can be selected by changing soldered wires. These changes should only be made by qualified technicians, to minimize the possibility of damage to the equipment.

Keyboard Bit 8. In standard factory-wired Terminals, the keyboard is wired so that a true bit 8 will accompany all characters which are entered at the keyboard. (The final determination of what is sent is made by the interface.) If a false bit 8 transmission is desired instead, the white-brown-blue wire on Pin 5 of plug P80 can be unsoldered and moved to pin 8 of P80. (P80 is the board-edge connector on the keyboard's circuit board.)

Control Characters. In standard factory-wired Terminals, control characters cause effects as listed in the Controls Section of this manual. A network on the TC-1 circuit card in the pedestal permits changes to be made so that any one of the listed results can be obtained in response to any one of the listed control characters. The networks are shown in Fig. 3-2.



(A.) Standard factory-wired configuration. Unlabeled lines are inputs, power or ground connections.

(B.) An example of rewiring, making EOT control the BEL line, rather than having BEL do it.

Fig. 3-2. TC-1 Control character network details.

It is not recommended to have one control character control more than one output line; nor is it recommended to have more than one control character control the same output line. Each of these last two conditions requires special design considerations.

TROUBLESHOOTING INFORMATION

Troubleshooting of the Terminal can be done best if the various features of this manual are used to their fullest advantage. These features and recommended usage are listed here.

Controls and Operation. This information insures operator understanding of the Terminal features and operation.

Specification. A complete explanation of the Terminal capabilities is contained in the Specification, along with explanations of how to put the capabilities into use.

Performance Check. This provides a rapid means of checking for proper operation in a logical sequence under normal equipment configuration. It can also be used with the options and the interface unit removed, to indicate operating status of the basic Terminal.

Adjustment. The procedure follows a logical sequence of adjusting the basic Terminal (including verifying non-adjustable features).

Block Diagrams and Circuit Diagrams. These diagrams and their associated descriptions provide an understanding of Terminal operation on a circuit as well as component level. The information contained therein is essential to efficient location of trouble.

Component Layout Illustrations. These appear in the Diagrams section and can be used as aids for locating components.

Interconnecting Wire Lists. A listing of cables, jacks and plugs, as well as an explanation of their use, is provided at the beginning of the Diagrams section. Wire colors are also provided, using the standard code for resistors.

Semiconductor Information. An illustration of semiconductors appears near the beginning of the Diagrams section, and can be used for pin identification. An integrated circuit test clip is recommended for use in troubleshooting the in-line integrated circuits, since it makes their leads easily accessible.

Troubleshooting Procedure

To troubleshoot the basic Terminal, remove all accessory cards and the interface card. Then check operation by doing the Performance Check. Stop where the Terminal fails to respond properly, and troubleshoot the referenced area, using block diagrams, schematics, and associated descriptions. Replacement of suspected circuit cards is recommended as a fast means of confirming suspicions. If the Performance Check works satisfactorily in the basic Terminal, install option cards and the interface card one at a time and repeat the Performance Check until it fails. Then troubleshoot the last-inserted option card and the circuits with which it interacts.

Obviously, not all troubles can be high-lighted by the Performance Check or Calibration Procedure. However, they should prove beneficial in most cases, and should go a long way in guiding a technician to the trouble area.

Recommended Troubleshooting Equipment

A Logic Extender Card, Tektronix Part No. 067-0653-00, is an efficient tool for circuit analysis. This card can be used as an independent plug-in card to make all minibus signals available to the Technician, providing level indicators for most of the lines. In addition, it provides a feature for injecting high or low level logic signals into the signal lines. The card can also be used as an extender for other circuit cards, and then permits interruption of any or all signals to the card which is attached to it.

Another extender card is available under Tektronix Part No. 670-1739-00. This card can be installed into the minibus to make bus lines available at test points, and can also be used as an extender for cards installed in the minibus.

A −15 V to +400 V DC voltmeter and a 10 MHz frequency response oscilloscope are recommended test equipment for troubleshooting low-voltage and logic circuits. A −6000 V DC meter is required for troubleshooting the high voltage circuits.

WARNING

Dangerous voltages exist within the pedestal and display units. Normal electrical safety precautions should be observed at all times when working around exposed circuits within these units.

When troubleshooting the power supply circuits, a resistive dummy-load should be connected in place of the Terminal circuits. This avoids accidental damage to other circuits in the Terminal. Recommended loads are as follows:

Power Supply	Connector	Load
+15 V	J70	30 Ω, 15 W
−15 V	J73	30 Ω, 15 W
+5 V	J72	1 Ω, 50 W

DISASSEMBLY AND ASSEMBLY

Access to the Display Unit Circuitry

For access to the circuits within the display unit, remove the three screws at the top of the rear surface. Then lift the top panel up and forward.

The high voltage shield must be removed to obtain access to the majority of the circuits on the High Voltage and Z Axis circuit board. To remove it, first remove the left side panel (as viewed from the front). Then remove the three screws from the shield. Lift the shield out the side of the unit.

Keyboard Information

Perform the following procedure to get at the keyboard circuits:

(1) Remove the four screws from underneath the front of the keyboard.

(2) Remove the four screws which hold the graticule mask in place and remove the mask.

(3) Remove the two screws from the top-rear of the keyboard panel.

(4) Pull the keyboard forward and then up as far as the cables will allow. Then turn the keyboard over.

(5) The top surface of the circuit board can be accessed by removing the six screws which hold the keyboard assembly to the keyboard panel.

Key caps can be removed by pulling them directly away from the keyboard. Use of a large pair of tweezers or a forceps is recommended.

Keys utilize reed switches whose solder contacts are accessible on the underside of the keyboard circuit board. Once the wires are unsoldered, the reeds can be extracted through the holes. Reverse the procedure for replacement.

Groups of keys are installed in assemblies which can be removed once the nuts are removed from the underside of the circuit board.

Pedestal Information

Access. For access to the upper section, loosen the two top screws and swing the top half of the cover down. For total access, remove the four screws from the bottom of the front cover; then loosen the two top screws and pull the cover off the front. Note that the line fuse is located in a holder at the bottom of the cover.

Circuit Card Removal. All cards connected to the minibus portion of the motherboard are held in by friction.

Power Supply Removal. Remove the cables which connect to the power supply circuit board. Remove the power plug which is connected to the transformer assembly.

At the bottom-front within the pedestal, remove the two screws which fasten the power supply side panels to the bottom of the pedestal.

On the outside at the back of the pedestal, remove the two screws on each side of the power supply heat sink.

Withdraw the power supply out the back.

When re-assembling the power supply, refer to Table 3-1 for cable-connecting information.

Silicon Grease. Silicon grease is applied to both sides of the mica insulators used with the following components: Q510, Q515, Q520, CR502, CR503. In addition, silicon grease is applied between the heat sink and the mounting plate on Q75.

TABLE 3-1

Power Supply Plug Reference

P70—3 pin connector	3 brown on red wires
P71—5 pin connector	Pin 1—orange on red wire Pin 3—green on white wire Pin 6—black on white wire
P72—6 pin connector	4 black on red wires
P73—3 pin connector	3 black on violet wires
P74—1 pin connector	Violet on white wire
P75—10 pin connector	Pin 1—blue Pin 2—brown 7 black wires
P76—3 pin connector	Pin 1—red wire Pin 2—blue on white
P77—3 pin connector	Pin 1—brown on red wire Pin 2—green on white wire Pin 3—orange on red wire
P78—3 pin connector	1 brown on violet wire
P79—3 pin connector	Pin 1—brown on violet wire Pin 2—black on violet wire Pin 3—red on white wire

Power Transformer Information

The power transformer (located in the pedestal) can be wired for use with 115 V or 230 V nominal line voltage, and can be set for any of several ranges within the nominal setting.

Instructions for connecting the transformer are contained on the inside of the pedestal front panel and are not repeated here. Note that the line fuse must also be changed when shifting between 115 and 230 volt operation. Instructions for fuse changing are contained on the panel which covers the transformer assembly.

Display Filter Removal, Cleaning, Installation

Removal. Remove the CRT mask after removing the four screws from its corners.

Place a small piece of tape on the surface of the filter, outside of the display area. This will be used as a reference during replacement. If a new filter is to be installed, it will be used for comparison.

Remove the angle brackets from the top and the bottom of the filter, after removing the two screws from the ends of each.

Lift the filter out of the neoprene mounting ring. It may be necessary to use a thin-bladed device to aid in removal. Use caution to avoid scratching or breaking the filter.

Cleaning. Clean the face of the CRT and the under-side of the filter, using a soft cloth and a mild soap and water solution. Note that the under-side can be distinguished from the outer surface by the masking tape if the original is being re-installed. If the old filter is being replaced with a new one, the under-side can be determined by comparing it with the old filter. Note that less glare from reflected light is apparent on the outer surface than on the under surface of the filter.

Installation. Put the filter in place in the recess in the neoprene mounting ring. The outer surface should be flush with the edge of the frame when properly installed. It may be necessary to use a non-abrasive device (such as a toothpick) to work the filter into place.

Install the angle brackets and fastening screws.

Clean the outer surface of the filter, using a soft cloth and a mild soap and water solution.

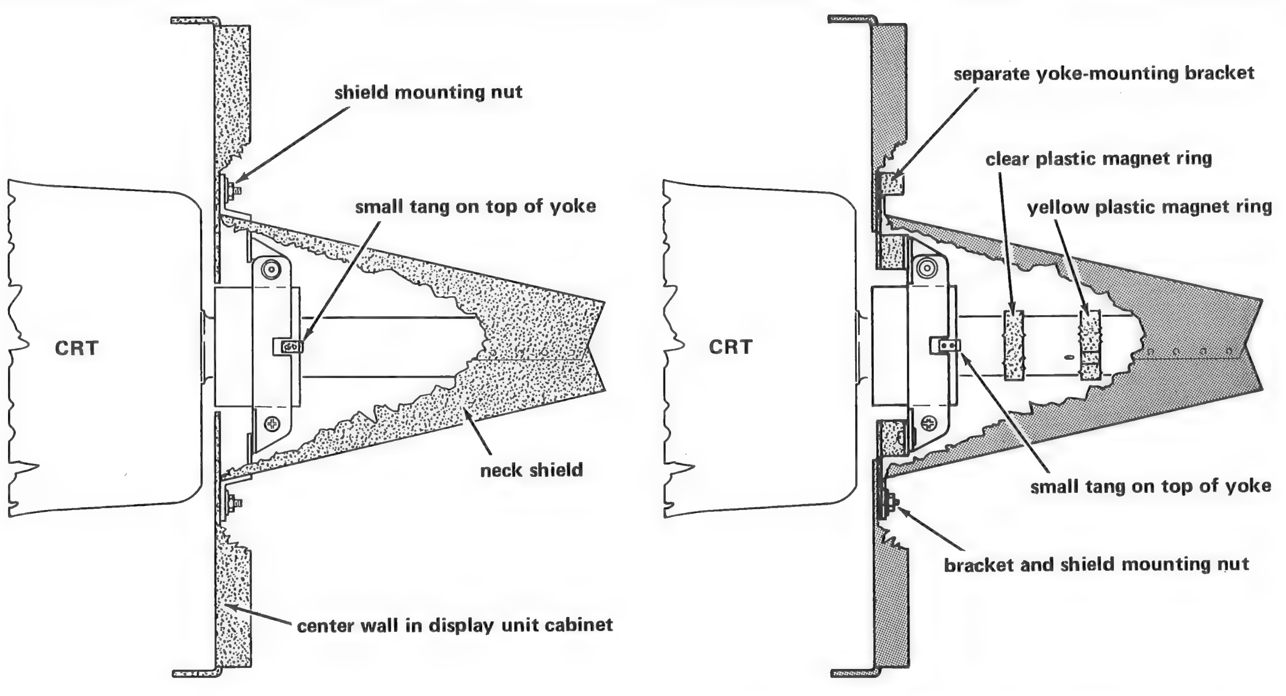
Install the face mask and fasten it in place with the four screws.

CRT and Deflection Yoke Removal and Installation

WARNING

The CRT may implode if it is scratched or struck severely. Do not handle the CRT by its neck. Wear protective clothing and a face shield when handling the CRT.

Introduction. There are two types of yoke-mounting hardware in use in the Terminal. The original type (integral yoke-mounting bracket) is shown in Fig. 3-3(A). Fig. 3-3(B) depicts the latest version (separate yoke-mounting bracket).



(A) Integral yoke-mounting bracket installation.

(B) Separate yoke-mounting bracket installation. Magnet rings may or may not be present; they should only be used when supplied with the CRT being installed.

Fig. 3-3. The two types of yoke-mountings.

CRT and yoke replacement procedures are considerably different for the two types. To determine the type being used, remove the top cover from the display unit cabinet and check for the presence or absence of the separate yoke-mounting bracket.

CRT Removal. Refer to the illustration in the Mechanical Parts List as necessary during this procedure. Remove the top from the display unit cabinet. Disconnect the plug from the rear of the neck shield by pulling gently and evenly on the leads. Disconnect the plug which connects to the bell end of the CRT. The connection may be at the top or bottom at the front of the neck shield.

Remove both side panels from the display unit after removing two screws from each.

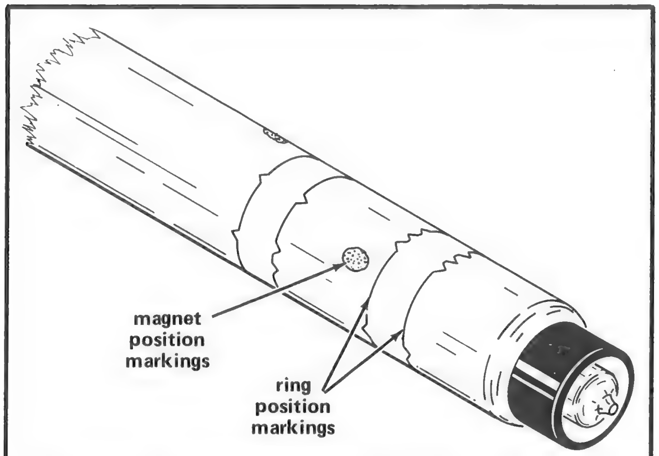
If the unit contains an integral yoke-mounting bracket, loosen the two nuts that fasten the neck shield to the center wall in the display unit, permitting the shield to move freely.

If a separate yoke-mounting bracket is installed, remove the rear panel from the display unit. Then remove the two nuts which hold the neck shield to the center wall. Remove the neck shield and replace (but don't tighten) the nuts, holding the yoke bracket in place. The CRT may or may not have one or two magnet rings installed on its neck. See Fig. 3-4. If rings are installed, note that the ring positions are marked as in Fig. 3-4(A), and then slide the ring(s) off the neck of the tube.

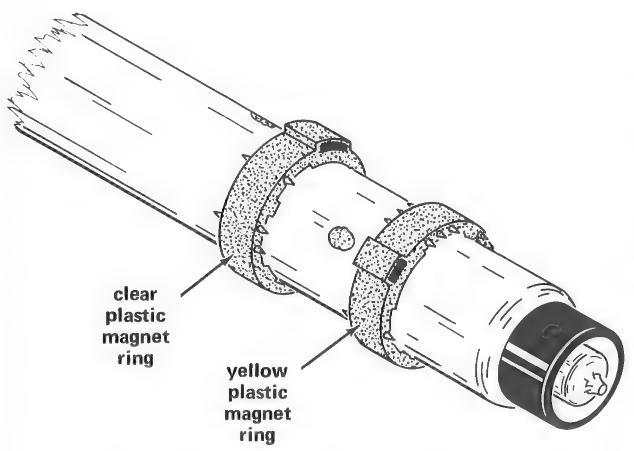
Remove the four screws which hold the CRT mask in place at the front of the display unit.

Place a small piece of masking tape on the front surface of the filter, outside of the CRT display area. It will be used for installation reference.

Remove the four nuts from the corners of the frame which holds the CRT in place. Then remove the frame and filter assembly from the front of the CRT. There are two types of frame assemblies in existence. The latest version has grounding clips fastened to each corner of the frame which holds the CRT in place. The clips are separate items in the early version, and may remain on the studs when the frame is removed; in this event, remove the clips before proceeding.



(A) Section of neck showing magnet ring position markings.



(B) Magnet rings installed. Note that magnets are aligned with dots on neck. Points on ring match points on position markings. Dots permit rapid locating of magnet position, but might not be present on all CRTs.

Fig. 3-4. CRT Magnet ring location details. The magnet rings should be used only when supplied with the CRT.

Slide the CRT out of the front of the unit, avoiding side pressure which may break the neck of the CRT. *DO NOT HOLD THE CRT BY ITS NECK.*

Set the CRT face-down on a flat surface. The neoprene mounting ring will keep the faceplate from contacting the surface.

Yoke Replacement. With the CRT removed, remove the nuts and washers which hold the neck shield or yoke-mounting bracket in place. Remove the shield or yoke-mounting bracket.

Unscrew the two bolts which fasten the yoke mounting strap to the shield.

Install the new yoke. Note that the metal tang fastened to the yoke is toward the top.

Install the yoke-mounting bracket or shield, as appropriate, in place on the center wall. Leave the nuts loose enough to permit the yoke to align with the neck of the CRT during replacement.

CRT Installation. Paragraphs prefaced "Replacement CRT Only" can be ignored if the previously-used CRT is being re-installed. Before proceeding, remove both side panels from the display unit after removing two screws from each.

Replacement CRT Only. Remove both side panels from the display unit after removing two screws from each.

On the right side (as viewed from the front), remove the four screws which hold the Deflection Amp & Storage board heat sink to the mounting panel (2 on top, 2 on bottom) below the circuit board. At each side, loosen (don't remove) two screws which hold the center wall in place, permitting the wall to be moved easily. Then position the wall so that the neoprene bumpers on the front of the CRT shield are just started past the tangs on the cabinet. Re-tighten the two screws at each side of the center wall.

Insert the CRT and attached neoprene mounting ring into the display unit cabinet, carefully aligning the neck with the yoke. Avoid side pressure on the neck. The plug connector can be either on the top or the bottom.

This paragraph pertains only to the early version of the frame assemblies in which the corner clips are separate from the frame. Remove the corner clips from the frame. Place a corner clip on each screw attached to the cabinet near each corner of the face of the CRT. The plane containing the hole should be outermost, with the clip aligning with the step in the neoprene mounting ring. See Fig. 3-5. (The clips may be difficult to align at this time, but will be adjusted as necessary in a later step.)

CAUTION

During the following procedure, the neck shield mounting nuts must be loose enough for the assembly to move easily, avoiding pressure on the neck.

Remove the filter and the two angle brackets from the frame. The angle brackets are held in place by screws at each end.

Put the frame in place, fitting it over the neoprene mounting ring. Install it carefully to avoid distorting the neoprene mounting ring. If necessary, slide the CRT forward slightly to make it easier to install the frame.

While holding the frame in place, install the four spacer sleeves over the corner screws, aligning the sleeves with the frame, clips, and screws as required. It may be necessary to lift up on the bottom of the frame. If the early version of the frame is installed, it may be necessary to adjust the clips while installing the spacers.

Start the nuts onto the top screws. Then place the nuts on the bottom screws, pressing in and up on the bottom of the frame as necessary.

If the early version of the frame is installed, check that the clips at the bottom corners are properly in place, extending over the step in the neoprene ring; then push each clip as far toward the corner as possible and tighten the bottom nuts. Repeat at the top corners. If the latest-version frame is installed (corner clips fastened to the frame), simply tighten the four nuts, drawing them up evenly.

Check the alignment of the CRT with the display unit cabinet. The edge of the display area should be parallel with the top edge of the display unit frame. If it isn't, loosen the corner nuts slightly, adjust the CRT, and retighten.

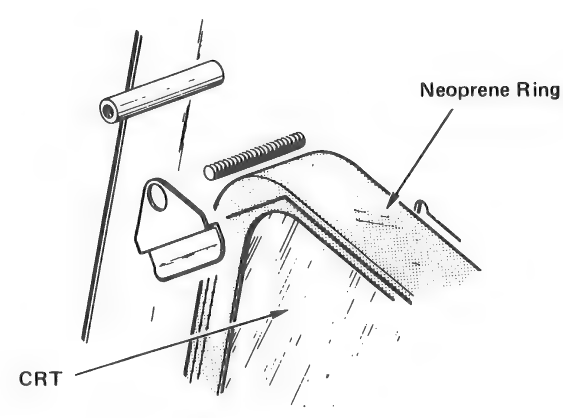


Fig. 3-5. Positioning of Corner Clips.

Using a soft cloth and a mild soap and water solution, clean the face of the CRT and the rear surface of the filter. (The rear surface is the side opposite to that having the tape attached. It can also be identified as the side exhibiting the most glare from reflected light.)

CAUTION

Avoid touching the face of the CRT or the back of the filter during the rest of the procedure. Otherwise, the filter will have to be removed for cleaning.

Set the filter in place in the recess in the neoprene mounting ring, with the side containing the masking tape on the outer surface. (The outer surface is the side exhibiting the least glare from reflected light.) The filter should fit flatly on all edges. Otherwise, it may break when tightened in place. When properly installed, the front surface of the filter should be approximately flush with the front surface of the frame. If it is not, it may be improperly seated in the neoprene ring. A toothpick, or other non-abrasive object may be used to move the lip on the neoprene ring sufficiently to allow the filter to move past the lip. If the early version of the frame is installed, a possible cause of improper seating could be that a corner clip may be mounted insufficiently far into the corner of the frame. In that case, loosen the appropriate corner screw, push the clip into the corner and retighten.

Put the angle bracket in place over the top and bottom edges of the filter, fastening them each in place with two screws. Note that filter breakage may occur if the front surface of the filter is not approximately flush with the front edge of the frame. Do not tighten just one screw at a time. Start all four screws and insert them evenly in small increments until all four are tightened.

Remove the masking tape which was put on for identification. Then clean the surface of the filter, using a soft cloth and a mild soap and water solution.

Put the face mask in place, and install the four screws.

Inside the unit, slide the deflection yoke mounting bracket or neck shield (as appropriate) up against the center wall and tighten the nuts which hold it in place.

Replacement CRT Only. Loosen the side screws which hold the center wall in place and slide the center wall forward, keeping the pressure in line with the neck of the CRT. Do not permit the center wall to move toward the back, or the shield may slip off of the tangs. *AVOID SIDE PRESSURE AGAINST THE CRT NECK.*

Tighten the side screws while holding the assembly in place.

This paragraph pertains only if the unit contains a separate yoke-mounting bracket. If magnet rings were supplied with the CRT, install them; align them as illustrated in Fig. 3-4. Remove the deflection yoke mounting bracket nuts. Slide the neck shield into place. Replace the nuts and tighten them moderately.

Replace the Deflection Amp & Storage board and attached heat sink, fastening it in place with the four screws.

Reconnect the CRT plug and the base plug. Note that they are both keyed for proper alignment.

Clean the front of the filter and replace the graticule mask, fastening it in place with the four screws.

Turn the Terminal on. After approximately one minute, press PAGE, put the rocker switch to LOCAL, and enter ESC and CTRL Z to obtain a crosshair display. Place the vertical thumbwheel at its upper limit, placing the horizontal line near the top of the display. Loosen the neck shield mounting screws sufficiently to permit moving the yoke-mounting bracket or shield. Then rotate the bracket or shield until the horizontal line is parallel with the top surface of the cabinet. Tighten the mounting screws. Fasten the rear cover, side panels, and top cover in place.

Turn the Terminal off. Fasten the top covers and the side panels in place.

PERFORMANCE CHECK/ADJUSTMENT

PERFORMANCE CHECK

General. This procedure can be used under normal operating conditions with all circuit cards installed. Since it uses LOCAL operation, no computer connection is required. Checks are referenced to a circuit and/or to a step in the Adjustment Procedure to permit rapid evaluation of incorrect results. In event of an improper response, recheck the step with all optional and interface cards removed from the pedestal to determine if the Terminal itself is at fault. Steps requiring position measurement should be made without parallax. That is, the line of sight should be perpendicular to the viewing area; this can be achieved by closing one eye and checking that the reflection of the viewing eye is in line with the point being observed.

Activity	Results	Circuit/Adjustment
Turn the Terminal on	Indicator on left of keyboard glows	Power Supply (Steps 1, 2, and 3)
Wait 30 seconds and then press PAGE	Erase cycle occurs	Storage circuits (step 6)
Wait 3 minutes and again press PAGE	Alpha cursor appears in top-left of display, approximately 1/4 inch from left edge and from top edge of display area	High Voltage and Z Axis circuits; Deflection circuits (steps 4 and 5) Terminal Control (TC) circuits; Cursor brightness (steps 7 and 8)
Wait about 2 minutes	Cursor disappears	View/Hold circuits
Press SHIFT	Cursor re-appears	View/Hold circuits
Select LOCAL; Hold 8 key down and enter about ten 8s.	8s are written in line and remain stored on display	Keyboard; Deflection circuits; Character Generator; Storage circuits (Step 6); Character brightness (steps 7 and 9)
Wait 5 minutes and press SHIFT	Check for fade-positive and drop-out effects	Storage circuits (Step 6)
Enter LINE FEED	With LF EFFECT option at LF, cursor moves vertically to next line; with LF EFFECT option at LF→CR, cursor moves to next line and to margin at left of display	TC
Enter 8s to complete a line (74 characters)	Cursor resets to next line and to margin at left of display	TC
Press PAGE	Erase cycle occurs; cursor goes home	TC

Activity	Results	Circuit/Adjustment
Enter 34 LINE FEEDs	Cursor goes to bottom-left corner of display	
Enter 35th LINE FEED	Cursor moves to Margin 1 position at top-center of display	TC
Enter thirty-seven 8s	8s written and stored; cursor moves to next line and back to Margin 1	TC
Enter 5 Space commands	Cursor moves 5 spaces to right	TC
Enter RETURN	With CR EFFECT option at CR, cursor moves to margin at center of display; with CR EFFECT option at CR→LF, cursor moves to margin at center of display and also moves vertically to the next line	TC
Check that the TTY LOCK key is released.	Check for proper writing and focus of ASCII characters	Keyboard; TC; Focus (step 10)
Enter each written character indicated on the keyboard, including shifted characters.	Characters are written on display	Keyboard; TC
Enter PAGE	Display erases; cursor goes home	
Press the TTY LOCK key to place it in its locked position. Press each character key with the SHIFT key released	All letters should be written upper case.	Keyboard
Enter ` { ¦ and ~	Note that they are inhibited. The code for the unshifted symbol is sent, regardless of the SHIFT key position	Keyboard
Press the TTY LOCK key	Lock releases	
Enter PAGE	Display erases; cursor goes home	
Enter ESC CTRL Z	Crosshair cursor appears but does not store	TC; Crosshair Cursor Intensity or Focus (steps 11 and 12)
Move vertical thumbwheel to upper limit	Horizontal line moves up near top of display; approximately 1/4 inch spacing exists between ends of line and edges of display area	

Activity	Results	Circuit/Adjustment
Move horizontal thumbwheel to mid-position	Vertical line is positioned near center of display; bottom of line should be approximately 1/4 inch from bottom edge of display area; horizontal line should be approximately 1/4 inch from top edge of display area	TC; Deflection Amplifier (Step 5)
Check horizontal line straightness	Distance between any point on the line and the mean path of the line should not exceed .03 inch.	Deflection Amplifier (Step 5)
Move vertical line to a position near the left edge of the display area (using the horizontal thumbwheel) and check vertical line straightness	All points should be within 0.5%. Distance between any point on the line and the mean path of the line should not exceed .04 inch.	Deflection Amplifier (Step 5)
Enter PAGE	Crosshair disappears, Alpha cursor appears at top-left corner	TC
Enter ESC CTRL Z	Crosshair returns	
Enter any key except PAGE or SHIFT RESET	No effect	
Position the crosshair intersection to approximate mid-screen and enter SHIFT RESET	Crosshair disappears and Alpha cursor appears at top-left corner	TC
Enter CTRL SHIFT M	Cursor disappears	TC
Enter Space ` Space @	Dark vector is executed; cannot be observed	TC
Enter @	Dot appears in lower-left corner	TC
Enter 8 k 8 K	45° diagonal line appears, starting from bottom-left corner	TC
Check line focus	Should be sharply focused	Step 10
Check line straightness	Distance between any point on the line and the mean path of the line should be within 2% (0.17 inch) of line length.	Step 14
Press PAGE	Alpha cursor appears at top-left	TC
Enter CTRL G (BEL)	Rings bell	TC
Enter TAB	Cursor moves one space to right	TC
Enter CTRL I (HT)	Cursor moves one space to right	TC

Activity	Results	Circuit/Adjustment
Enter BACKSPACE	Cursor moves one space to left	TC
Enter CTRL H (BS)	Cursor moves one space to left	TC
Enter LF	Cursor moves down one line; may also return to margin if the LF EFFECT option is at LF→CR	TC
Enter CTRL J (LF)	Cursor moves down one line	TC
Enter CTRL K (VT)	Cursor moves up one line	TC
Enter CTRL SHIFT M (GS)	Selects Graph Mode; cursor disappears	TC
Enter Space RUBOUT Space _ + RUBOUT Ø _	Vector appears	TC
Enter ESC CTRL W (ESC ETB)	Copy of display is made if Hard Copy Unit is attached and energized	TC; Hard Copy TARSIG Amp; Hard Copy Selector; High Voltage and Z Axis circuit; Storage circuit; steps 18 through 22
Enter ESC CTRL L (ESC FF)	Display erases; Alpha cursor homes	TC
Enter CTRL SHIFT M (GS)	Cursor disappears	TC
Enter @ @	Dot appears near display center	TC
Enter CTRL SHIFT O (US)	Alpha cursor appears with bottom-left corner at dot	TC
Enter CTRL SHIFT M (GS)	Cursor disappears	TC
Enter @ _	A line is written near display center	TC
Enter CTRL M (CR)	Alpha cursor appears at left margin opposite the line. If CR EFFECT strap is at CR→LF, the cursor will also move down one line.	TC
Enter CTRL SHIFT M Space Space DD	A dot should appear at bottom-left corner	TC
Enter CTRL SHIFT M 8 k ? _ _	A dot should appear at upper-right corner	TC
Enter ESC CTRL Z (ESC SUB)	Alpha cursor disappears; crosshair cursor appears (should not be entered at keyboard with switch at LINE)	TC
Using thumbwheels, move intersect point to dot at bottom left of display	Intersect point is positioned to 4X, 0Y	TC

Activity	Results	Circuit/Adjustment
Move intersect point to dot at top right of display	Intersect point is positioned to TC 1023X, 779Y	
Press PAGE	Display erases; Alpha Mode is reset; Alpha cursor goes home. Performance check completed.	

ADJUSTMENT

Introduction

Adjustment of the Terminal normally is required only when it ceases to properly perform its intended functions, or after circuit repairs have been made. However, if adjustment is to be performed on a routine schedule, an interval of one year between adjustments is recommended. Adjustment should be preceded by a thorough cleaning and inspection as outlined in the Servicing section. Adjustment should be performed in a +20°C to +30°C environment and should be preceded by a thirty minute warmup period.

Equipment Required

The following equipment is required in this procedure: Variable voltage source which has an output capability of at least 2 A at 100, 110, or 120 VAC, or at least 1.25 A at 200, 220, or 240 VAC. The instrument output should be variable to at least plus and minus 10% from the stated value.

Oscilloscope. Dual trace with vertical deflection factors of 5 mV, 0.5 V, and 2 V per division, and sweep rates of 0.1 μs, 0.5 μs, 1 ms, and 10 ms per division; frequency response should include DC to at least 10 MHz.

Voltmeter. Range at least −25 V DC to +400 V DC; accuracy within at least .05% at +15 V, 0.1% at −15 V, 0.2% at +5 V, and at least 1% at all other voltages. High voltage range to −6000 V DC, accurate to within at least 0.5% at −5850 V DC.

Integrated Circuit Test Clip, or 72 Pin Extender Card (Tektronix Part No. 670-1739-00), **or Logic Extender Card** (Tektronix Part No. 067-0653-00). Needed for connecting TSTROBE to CSTROBE. If the Integrated Circuit Test Clip is used, one clip is required if a TTY Port Interface or an 021-0065-00 Data Communication Interface is installed; two clips are needed if an Optional Data Communication Interface is installed.

Screwdriver. 1/8 inch tip; non-conductive, at least ten inches overall length.

Hard Copy Unit. Used for adjusting copy-making circuitry, which must be adjusted only if the Terminal will be used with a Hard Copy Unit.

Index of Adjustments

The following can serve as an index, or as an adjustment record. It can also be used as a short form adjustment procedure for technicians experienced in adjusting the Terminal. If used as a record of adjustment, copies should first be made to avoid writing on the copy in the manual.

Date adjusted: ____________ By: ____________________

See Tables 4-1 and 4-2 for details.

2. +5 V Over-Voltage Check/Adjustment (R50, Crowbar on Power Supply Board in pedestal) — Page 4-12

Adjust R50 for 4.8 V at Q99 base. Short R26-R27 junction to R43-C43 junction to open F41. Replace F41 with 6 A fast-blow fuse.

3. High Voltage Check/Adjustment (R227, HV on High Voltage & Z Axis Board in display unit) — Page 4-13

Adjust R227 for —5850 V at TP45.

4. Pre-adjust Writing Intensity, Focus, and Alpha Cursor Brightness (FOCUS ADJUST and R86, Writing Intensity on High Voltage & Z Axis Board in display unit; Alpha cursor Brightness on TC-1 in pedestal) — Page 4-13

With Cursor Brightness on TC-1 fully CW, adjust R86 until no dot appears after an erase cycle; adjust Cursor Brightness on TC-1 for minimum brightness consistent with good viewing; adjust FOCUS ADJUST for focused cursor.

5. Display Positioning Check/Adjustment (X GAIN, Y GAIN, X POS, Y POS, X GEOM, Y GEOM on Deflection Amp & Storage Board in display unit) — Page 4-14

Adjust R29 (R85 on boards numbered 670-1729-04 and below), Crosshair Brightness on TC-2 for nonstoring cursor. Adjust X POS to center horizontal GIN line; with vertical thumbwheel at upper limit, adjust Y POS so horizontal line is the same distance from the top of the display area as the bottom of the vertical line is from the bottom of the display area; rotate neck shield or yoke-mounting bracket for parallelism between horizontal line and top of display area; adjust X GEOM for straight vertical line; with horizontal line near top of display, adjust Y GEOM for straight horizontal line; adjust X GAIN for 7.9 inch horizontal line; adjust Y GAIN for 6 inches between bottom of vertical GIN line and top of top line of Alpha Mode characters.

6. Storage Check/Adjustment (NORM COLL, OP LEVEL in Deflection Amp & Storage Board in display unit) — Page 4-16

Adjust NORM COLL for presence (at Deflection Amp & Storage Board J55 Pin 3) of CE value written on shield; adjust OP LEVEL for presence (at Deflection Amp & Storage Board J55 Pin 4) of STORAGE LEVEL value written on shield for same CRT, or to value midway between fade-positive and drop out for replacement CRT. Re-adjust OP LEVEL as necessary to avoid fade-positive after erase cycle, or drop out from fully written page. Re-adjust NORM COLL for optimum uniformity and brightness.

7. Writing Intensity Check/Adjustment (R86, Writing Intensity on High Voltage & Z Axis Board in display unit) — Page 4-18

Adjust R86, Writing Intensity for complete vectors drawn by the following commands:

Space ` Space @ 8 k ? _ 8 k Space @ Space ` ? _ 8 k ? _

8. Alpha Cursor Brightness Check/Adjustment (R81, Alpha Cursor Brightness on TC-1 in pedestal) — Page 4-20

Adjust R81 for desired non-storing Alpha cursor intensity.

9. Alpha Character Brightness Check/Adjustment (R74-Character Brightness on TC-1 in pedestal) — Page 4-20

Adjust R74 for desired brightness of Alpha Mode characters.

10. Character and Vector Focus Check/Adjustment (FOCUS ADJUST and R389, Character/Vector Focus Adjust on High Voltage & Z Axis Board in display unit) — Page 4-20

Adjust FOCUS ADJUST for best focus of an e character in top-left corner of display. Compromise for sameness in four corners of display area. Adjust R389 for similar focus of e near center of display.

11. Crosshair Cursor Intensity Check/Adjustment [R29 (R85 on boards numbered 670-1729-04 and below), Crosshair Cursor Brightness on TC-2 in the pedestal]. — Page 4-21

Adjust R29 (R85 on boards numbered 670-1729-04 and below) in GIN Mode so that the cursor is visible but does not store.

12. Cursor Focus Check/Adjustment (R382, Cursor Focus on High Voltage & Z Axis Board in display unit) Page 4-21

With crosshair displayed, intersect near screen center, adjust Cursor Focus for optimum overall focus.

13. Vector Drawing Time Check Page 4-21

2.6 ms negative-going pulse at J49 pin 1 on Deflection Amp & Storage Board following entering of the underline symbol while in Graph Mode.

14. Vector Dynamic Geometry error check Page 4-21

Check that separation between vectors does not exceed 1/4 inch after entering following commands in Graph Mode:

Space ` Space @ 8 k 8 K Space ` Space @

15. Vector Parallelism Check Page 4-22

Enter Space ` Space @ 8 k @ k ? _ Space ` _ ` Space @ and then check that the difference between lengths of the horizontal lines does not exceed 0.16 inch, and that the difference between lengths of the vertical lines does not exceed 0.12 inch.

16. Character Transmission and Writing Check Page 4-22

Check writing of each ASCII character; check that TTY LOCK restricts transmission to TTY code.

17. Control Character Transmission and Response Check Page 4-22

Check control character response as outlined in step 17 of the detailed procedure.

18. Hard Copy position and Amplitude Check/Adjustment (HC X AMP, HC Y AMP, FAST RAMP POS, SLOW RAMP POS on Deflection Amp & Storage Board in Display Unit) Page 4-23

Adjust SLOW RAMP POS and HC Y AMP for scan 1/4 inch below and 1/8 inch above page full of written characters; adjust FAST RAMP POS and HC X AMP for scan 1/8 inch beyond left and right edges of page full of written characters.

19. Hard Copy Intensity Adjustment (R91, Coarse Hard Copy Intensity on the High Voltage & Z Axis Board in the display unit, and Hard Copy Intensity on the side of the display unit) Page 4-25

With the external Hard Copy Intensity adjustment at mid-range position, adjust the coarse Hard Copy Intensity (R91) just below the level at which the Hard Copy scan bar stores.

20. Hard Copy Threshold Check/Adjustment (R167, Hard Copy Threshold on Hard Copy Amplifier Board in display unit) Page 4-25

Adjust R167 so that pulses observed at TP85 and TP195 are almost touching during hard copy scanning. Oscilloscope at 0.5 μs and 0.5 V per division.

21. Hard Copy Dynamic Threshold Adjustment (R265, Hard Copy Dynamic Threshold on Hard Copy Amplifier board in display unit) Page 4-26

Adjust R265 so separation between waveforms remains fairly constant during hard copy scanning. Oscilloscope at 1 ms and 0.5 V per division.

22. Hard Copy Writing Check Page 4-27

Check for five sequential satisfactory copies of the same display. Re-adjust Hard Copy Intensity if necessary.

23. Restoring Original Conditions Page 4-28

Turn Terminal off; remove line plug; reset transformer wiring and fuse; reset option straps; remove the Extender Card or IC Test Clip(s). Remove jumper(s) (on J360 on 021-0065-00 Interface; on J161 and J162 on TTY Port Interface). Reconnect output cable or reset the control switch (cable on 021-0065-00 or TTY Port Interfaces; switch on 021-0074-00). Replace the covers.

Preliminary Procedure

Turn off the Terminal power switch (at top of pedestal) and remove the line cord from the power source.

WARNING

Dangerous voltages exist within the Terminal display unit and pedestal. Normal electrical precautions should be observed whenever working within those units while the covers are removed.

Although the Terminal can be adjusted without separating the display unit and pedestal, it is much more convenient if they are separated and placed alongside each other on a work bench. To separate them, remove the four screws which hold the display unit to the pedestal. The screws are located underneath the display unit mounting plate which is on top of the pedestal. (Refer to the mounting procedure illustration in Fig. 3-1, if necessary.) Support the front of the display unit while the last screw is being removed. Then move the display unit back about 1/2 inch and lift up on it. Withdraw enough cable from the top of the pedestal to permit the display unit to be set down on a bench adjacent to the pedestal as shown in Fig. 4-1.

Remove the three screws from the back of the top cover on the display unit. Remove the cover by lifting the back of it up and forward.

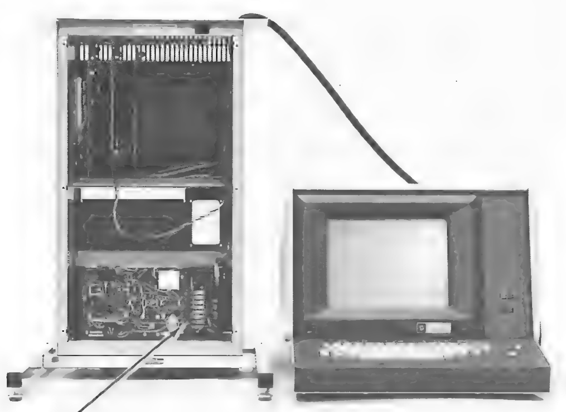


Fig. 4-1. Setup for Adjusting.

Remove the two middle and two bottom screws from the pedestal's front cover. Then unscrew the two thumbscrews from the top of the front cover and remove it. The fuse is mounted in a holder in the bottom of the front cover and is removed with the cover.

This procedure does not include accessory cards which may be used with the Terminal (such as Display Multiplexer or Audio Recorder Interface). Therefore, remove all cards other than TC-1, TC-2, and the Communication Interface Card from the top section of the pedestal.

Pull TC-1 and TC-2 out and check the strap options shown in Fig. 4-2. TC-1 can be identified by the two adjustments on the front edge, near the top. TC-2 has an adjustment and a cable connection near the front-bottom corner. If the strap option positions must be changed, record their original positions and change them to agree with Fig. 4-2. Then install the cards in the minibus.

Determine the type of Interface card installed. If it is a Data Communication Interface 021-0065-00, check it against Fig. 4-3 and change the straps as necessary, recording the original setting. Then disconnect the cable from J360 and strap J360 pin 1 to J360 pin 7 on the card. Connect $\overline{\text{T STROBE}}$ to $\overline{\text{C STROBE}}$; an extender card can be placed between the minibus and the circuit card, and minibus pin 3 connected to minibus pin 5; or U67 pin 10 can be connected to U67 pin 11 on the 021-0065-00 Data Communication Interface card by first connecting an Integrated Circuit Test Clip to U67. Install the Interface card in the minibus.

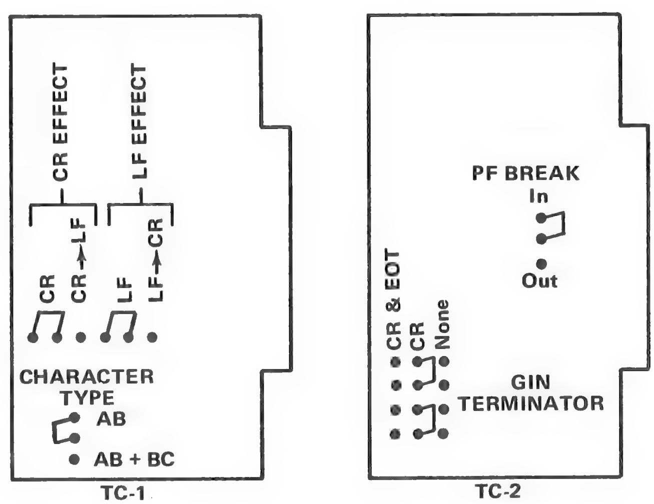


Fig. 4-2. TC-1 and TC-2 strappable option selections for adjusting the terminal.

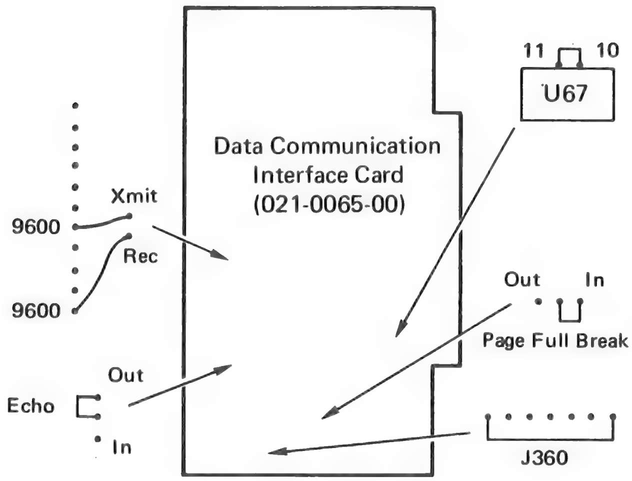


Fig. 4-3. Data Communication Interface (021-0065-00) strappable option and jumper positions for adjusting the terminal.

If the Interface is an Optional Data Communication Interface 021-0074-00, set the selector switch (rear panel) to the LOOP BACK position. Set the TRANSMIT BAUD RATE switch and the RECEIVE BAUD RATE switch both to 9600. (Record the previous positions for later reference.) Connect $\overline{\text{T STROBE}}$ to $\overline{\text{C STROBE}}$ either by using an extender card and connecting minibus pin 3 to 5, or by using two integrated circuit test clips and connecting U68 pin 6 to U47 pin 9. Install the Interface Card in the minibus.

If a TTY Port Interface is installed, disconnect the Relay Card cables from the J161 and J162 connectors on the Control Card. Set the card straps as shown in Fig. 4-4. Record the original positions of any straps that have to be changed. Connect J162 pin 2 to J162 pin 3; connect J161 pin 6 to J162 pin 7. Connect $\overline{\text{T STROBE}}$ to $\overline{\text{C STROBE}}$, either by using an extender card and connecting minibus pin 3 to pin 5, or by using an integrated circuit test clip and connecting U81 pin 3 to U81 pin 6. Install the Interface Card in the minibus.

CAUTION

Do not put the Terminal in Graph Mode at any time while the $\overline{\text{T STROBE}}$ to $\overline{\text{C STROBE}}$ strap is connected.

At the lower right corner of the pedestal, remove the shield which covers the transformer terminals (see Fig. 4-1). It is held in place by two screws on top. Determine what voltage the transformer is wired for, by comparing the connections against the diagram on the inside surface of the pedestal cover. If a variable AC power supply is available, it will be set to that value. If the indicated supply is not available, record the transformer wiring condition so that it can be restored upon completion of the adjustment procedure. Then rewire the transformer connections to agree with the available voltage supply. See diagram inside the front cover for instructions.

Install an appropriate slow blow fuse (2 A for 115 V or 1.25 A for 230 V) and replace the shield to minimize shock danger. If the fuse mounted in the front cover is to be used during the adjustment, it can be pushed (not pulled) from its holder, or the holder assembly can be removed from the front cover, as desired.

WARNING

Dangerous voltages exist in the fuse and transformer circuits. Keep the line cord disconnected while working in those areas.

Check the remaining fast blow fuses for proper sizes. Their values should be: F21—2 A, F41—6 A, F61—2 A.

Detailed Procedure

1. Low Voltage Power Supply Check/Adjustment (R27, Reg Voltage on Power Supply Board in pedestal)

a. After the preliminary procedure has been completed, connect the line cord to a variable power source (autotransformer) which is set to the voltage for which the transformer is wired.

b. Turn the Terminal power switch ON and place the LOCAL/LINE switch at LOCAL.

c. Connect the voltmeter reference lead to the ground point shown in Fig. 4-5.

d. Using a voltmeter which has .05% or better accuracy at 15 V, adjust R27 to obtain +15.000 V at the +15 V test point. Adjustment and test point locations are shown in Fig. 4-5.

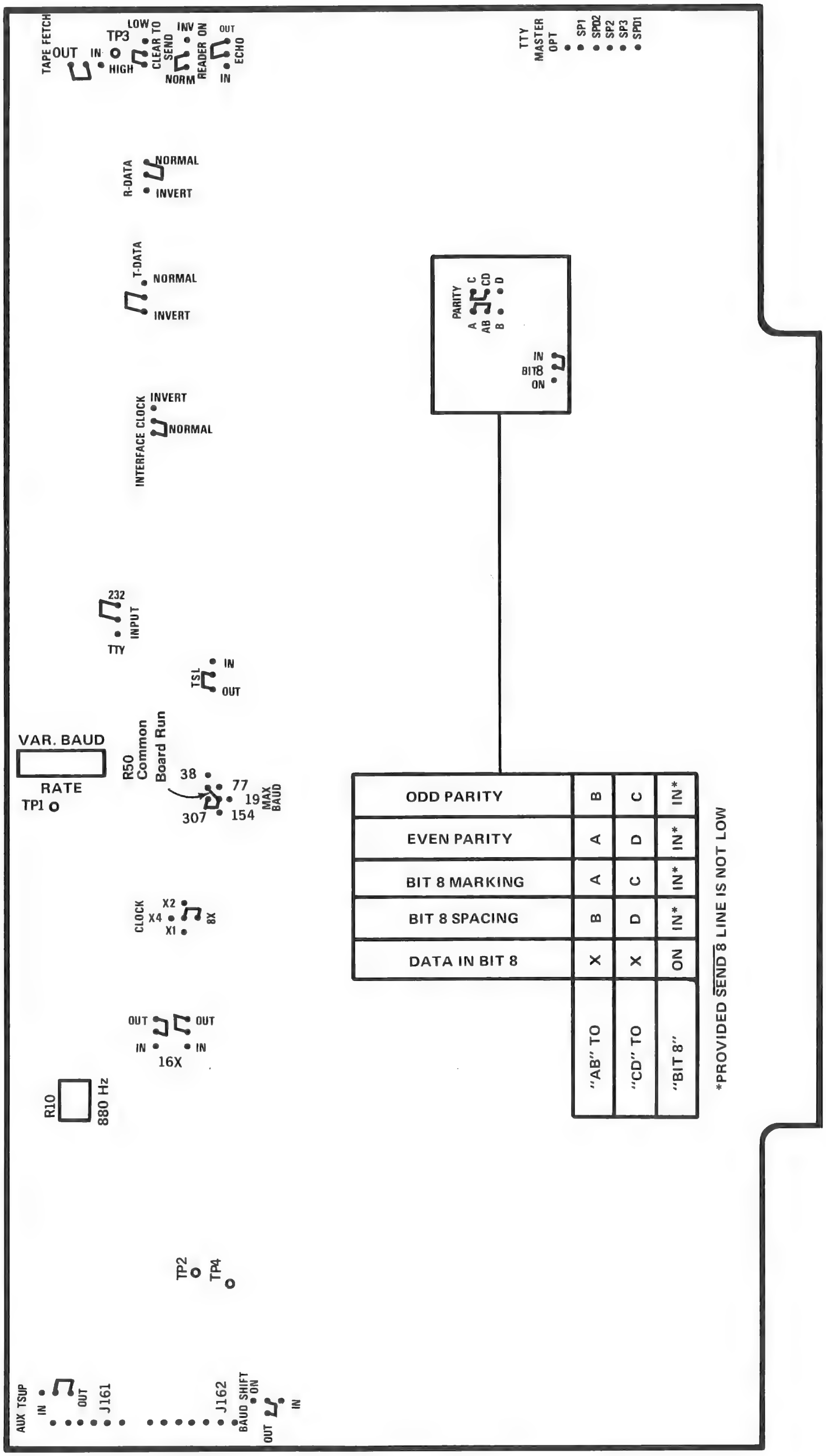


Fig. 4-4. TTY Port Interface strap option position for calibrating the Terminal.

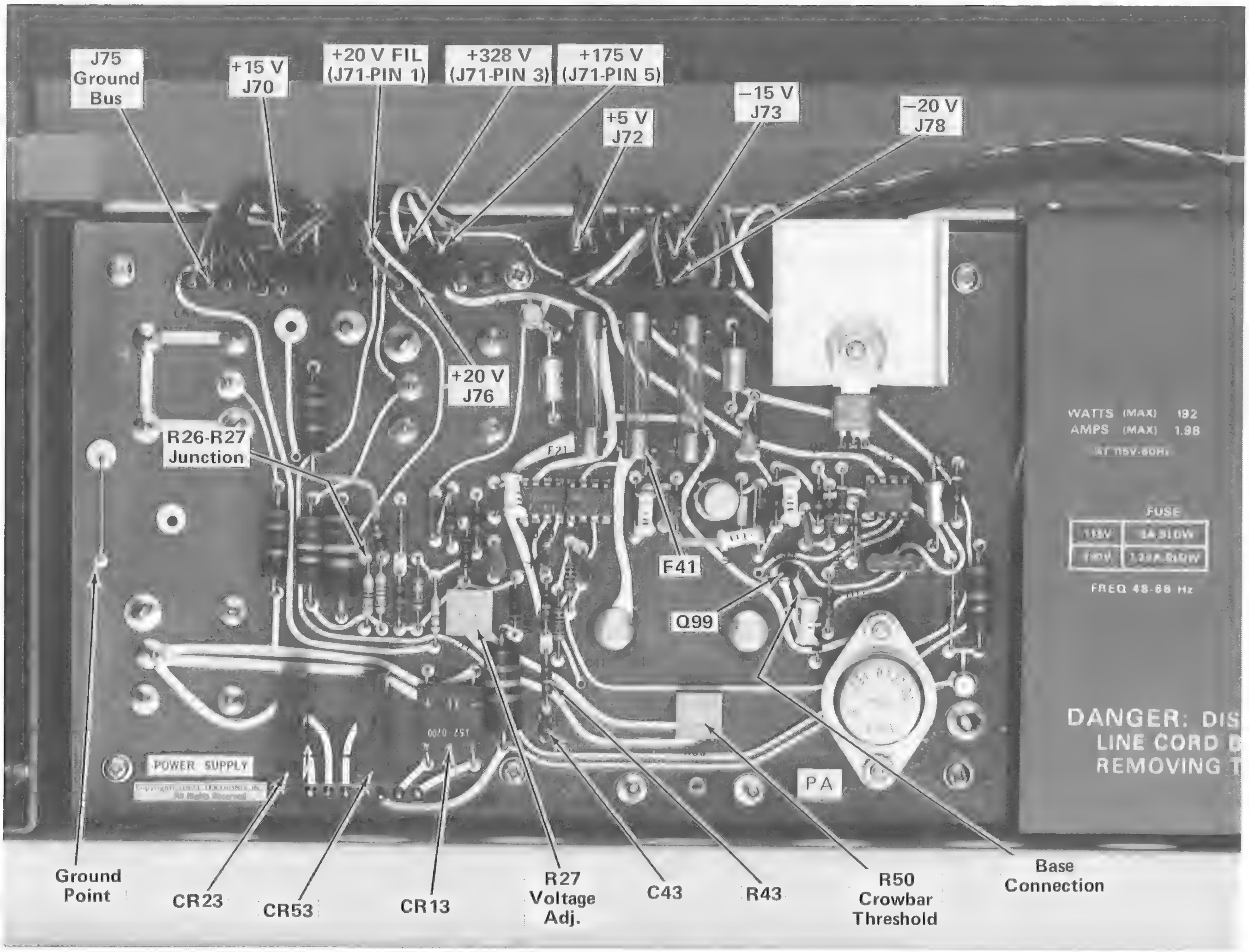


Fig. 4-5. Power Supply Adjustments and Test Points.

e. Measure the various power supply voltages as listed in Table 4-1. Test points are shown in Fig. 4-5. Record all voltages in Table 4-2. (Make duplicate copies of Table 4-2 for future use.)

f. Using the test oscilloscope, check that ripple voltages do not exceed those values given in Table 4-1. If ripple appears excessive or marginal, move the voltage reference lead to the ground bus at J75 and recheck.

g. Change the variable power source to 10% below the center value for which the transformer is wired.

h. Measure and record the supply voltages, again using Tables 4-1 and 4-2. Then check the ripple of each supply.

i. Change the variable power source to 10% above the center value for which the transformer is wired.

j. Again measure and record the supply voltages and check ripple.

k. Analyze the results. All voltages should be within the specified values. The differences between voltages at center line and either high or low line should not show a regulation factor larger than that specified in Table 4-2.

l. Set the line voltage to the center voltage for which the transformer is wired.

TABLE 4-1

Power Supply Voltage Limits

Supply	Jack	Voltage Limits	Ripple (P-P)	Comments
+15 V	J70	+14.025 to +15.075	10 mV	Adjust R27 for +15.000 V; readjust if necessary to compromise so that +15, +5, and −15 V supplies are all within limits with line voltage at mid-position as well as at high and low limit.
+5 V	J72	+4.9 to +5.1	10 mV	
−15 V	J73	−14.850 to −15.150	10 mV	
−20 V Unreg	J78	−20.0 to −22.5	2.8 V	Not adjustable
+20 V Unreg	J76	+20 to +22 5	2.8 V	
+20 V Fil	J71-1	36 to 44 V more positive than −20 V Supply	2.8 V	
+175 V Unreg	J71-5	+163 to +176	6 V	
+328 V Unreg	J71-3	+317 to +330	8 V	

TABLE 4-2

Observed Voltages

Supply	(A) Center Line Voltage	(B) Low Line Voltage	(C) High Line Voltage	(D) Greater Deviation From (A)	% Observed Regulation $\frac{(D)}{(A)}$ X100	Regulation Limit
+15 V						0.2%
+5 V						1.0%
−15 V						0.2%
−20 V Unreg				NOT APPLICABLE		
+20 V Unreg						
+20 V Fil						
+175 V Unreg						
+328 V Unreg						

2. +5 V Over-Voltage Check/Adjustment (R50, Crowbar on Power Supply Board in pedestal)

a. Check the voltage at the base of Q99 for 4.8 V. Adjust R50 as necessary to obtain that value. See Fig. 4-5 for component locations.

b. Check over-voltage protection. A spare 6 A fast-blow fuse is needed for this check. If none is available, this step will have to be omitted.

(1) Using a shorting strap, momentarily connect the R26-R27 junction to the R43-C43 junction, expecting a

flash from F41. See Fig. 4-5 for locations. The voltage at the +5 V test point indicated in Fig. 4-5 should drop to 0 V.

(2) Turn the Terminal power switch OFF and disconnect the line cord.

(3) Replace F41 with a new 6 A fast-blow fuse. (If F41 does not open, troubleshoot the power supply. All plugs should be removed from the board and dummy loads substituted during troubleshooting; logic circuitry may otherwise be damaged. Instructions are given in the Maintenance Section. Check plug locations before removing, to insure their proper replacement.)

c. As a precautionary measure, the front cover may be replaced at this point, and the top half swung down on its hinge. This will cover the Power Supply while still permitting access to the circuits in the top half of the pedestal. Note that the line fuse clip in the pedestal must be empty and a proper sized fuse (2 A for 115 V, 1.25 A for 230 V) must be installed in the cover prior to cover replacement.

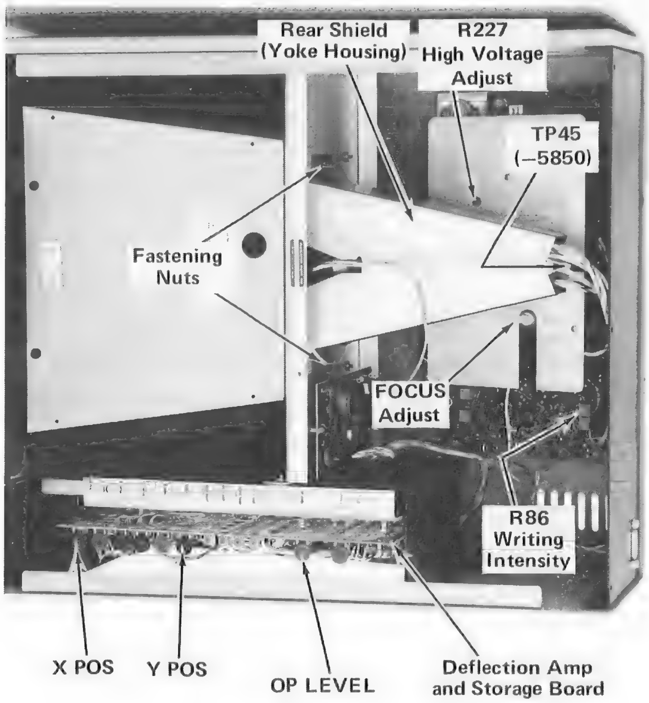


Fig. 4-6. High Voltage Adjustments and Test Points.

3. High Voltage Check/Adjustment (R227, HV on High Voltage & Z Axis Board in display unit)

a. With the Terminal off, set the voltmeter to read −5850 V DC and connect it to TP45 on the High Voltage & Z Axis board in the back of the display unit. See Fig. 4-6.

b. Reconnect the line cord and turn the Terminal power switch ON.

c. After about one minute, press PAGE. Then check for −5850 V at TP45. Adjust R227, High Voltage Adjust (Fig. 4-6) as necessary to obtain that value. Use a non-metallic screwdriver to minimize the possibility of causing a short circuit.

d. Set the variable power source first to 10% below the transformer center voltage and then to 10% above it and check that the high voltage remains between −5557 and −6143 volts at both positions.

e. Set the variable power source to the transformer center voltage.

f. Turn the Terminal power switch OFF.

g. Disconnect the voltmeter from TP45.

4. Preadjust Writing Intensity, Focus, and Alpha Cursor Brightness (FOCUS ADJUST and R86, Writing Intensity, on High Voltage & Z Axis Board in display unit; Alpha Cursor Brightness on TC-1 in pedestal)

a. In this and subsequent steps employing Alpha Mode, the Terminal may go into Hold status, diminishing display brightness. Entering any character will restore the View status; however, pressing the SHIFT key will restore View status without otherwise affecting the display.

b. Turn the Terminal ON and after approximately one minute, momentarily press the PAGE key to initiate an erase cycle.

c. Note the edges of the display area after the erase cycle has been completed. If the edges become obviously brighter than the rest of the display area (fade-positive, Fig. 4-10), turn the OP LEVEL (on Deflection Amp &

Storage board, Fig. 4-6) fully counterclockwise. (OP LEVEL will be adjusted properly in a later step.)

d. At TC-1 in the top of the pedestal unit, turn R81, Alpha Cursor Brightness, fully clockwise. (See Fig. 4-7 for location.)

e. Enter 37 space commands and 17 LF commands.

f. On the High Voltage & Z Axis board in the back of the display unit, rotate R86 Writing Intensity (Fig. 4-6) to increase intensity until the Alpha cursor can be seen near the center of the display. Do not make the cursor any brighter than is necessary. If the Alpha cursor doesn't appear, R81 on TC-1 may be set to the wrong limit, or the Terminal may be in Hold status. (Press SHIFT to clear Hold status.)

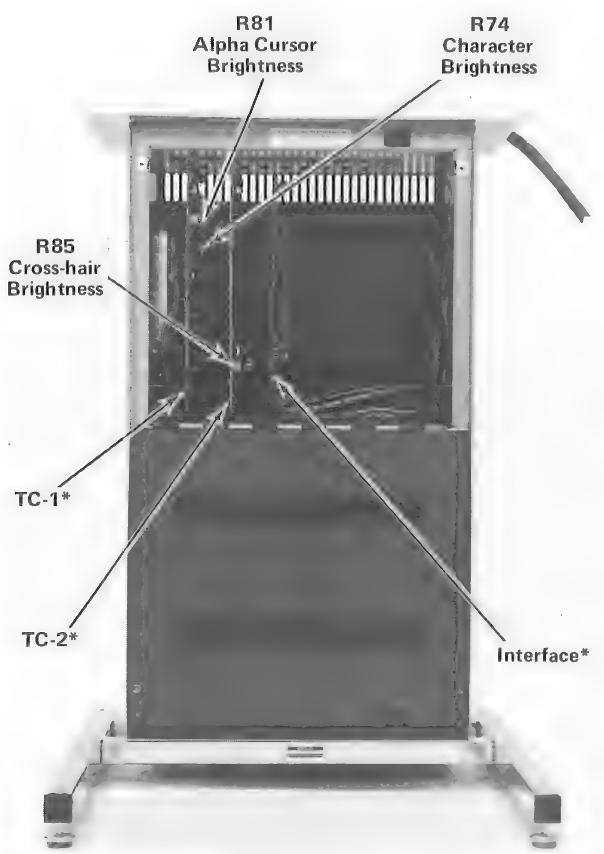


Fig. 4-7. Pedestal Circuit Card Information.

g. Press PAGE. The cursor should move to the top-left corner of the display. If the cursor was viewable in step f, and now has moved entirely out of the viewing area, turn X POS fully counterclockwise and Y POS fully clockwise to bring the cursor back into view. X POS and Y POS are located on the top of the Deflection Amp & Storage board in the display unit. See Fig. 4-6.

h. Press PAGE and check for the momentary appearance of a dot at the bottom-left of the cursor position. The dot may appear just before the cursor comes back into view. Adjust R86 (Fig. 4-6) until a dim dot momentarily appears at the bottom-left corner of the cursor position after the erase cycle, as just described. Then readjust R86 just to the point where the dot no longer appears after an erase cycle. The cursor should still be visible.

i. At TC-1, adjust R81, cursor brightness (Fig. 4-7) until the cursor is at minimum brightness consistent with good viewing.

j. Adjust FOCUS ADJUST on the High Voltage & Z Axis board in the display unit (Fig. 4-6) to obtain a reasonably focused cursor. (Final focusing will be done later in the procedure.)

5. Display Positioning Check/Adjustment (X GAIN, Y GAIN, X POS, Y POS, X GEOM, Y GEOM on Deflection Amp & Storage Board in display unit)

NOTE

This procedure provides for an approximately centered display of specific size. Both positioning and size may be modified as desired by changing the adjustment parameters accordingly. All position and size measurements should be made with a minimum of parallax. This can be achieved by closing one eye and keeping the reflection of the viewing eye in line with the point being observed.

a. Enter ESC and CTRL Z and place the keyboard thumbwheels near midrange. A crosshair cursor should appear on the display. If it does not, or if it is excessively bright, adjust R29 [Crosshair Brightness (R85 on boards numbered 670-1729-04 and below)] on TC-2 as necessary to provide a display of minimum intensity, consistent with

good viewing. The crosshair should not be so bright that it stores; move the thumbwheels to check for storing. The R85 location is shown in Fig. 4-7.

b. Put the vertical thumbwheel to its upper limit.

c. Enter PAGE and ESC and CTRL Z to erase the display and regain the crosshair. (ESC and CTRL Z must be entered to regain the crosshair cursor each time the display is erased, since PAGE also resets the Terminal to Alpha Mode.)

d. Check display positioning. It should meet the following requirements (see Fig. 4-8):

Horizontal line	Should remain in view
	Both ends occur before reaching edges of display area
	Approximately centered horizontally in display area
	Approximately 7.9 inches long
	Parallel with top edge of display area
	Distance between any point on the line and the mean path of the line should not exceed .04 inch (0.5% of line length).
Vertical line	Bottom end occurs approximately 0.5 inch before reaching edge of display area
	Horizontal intercept is approximately 6.0 inches above bottom of vertical iine
	Approximately parallel with left edge of display area
	When positioned near left edge of display area (by using horizontal thumbwheel), distance between any point on the line and the mean path of the line should not exceed .03 inch (0.5% of line length)

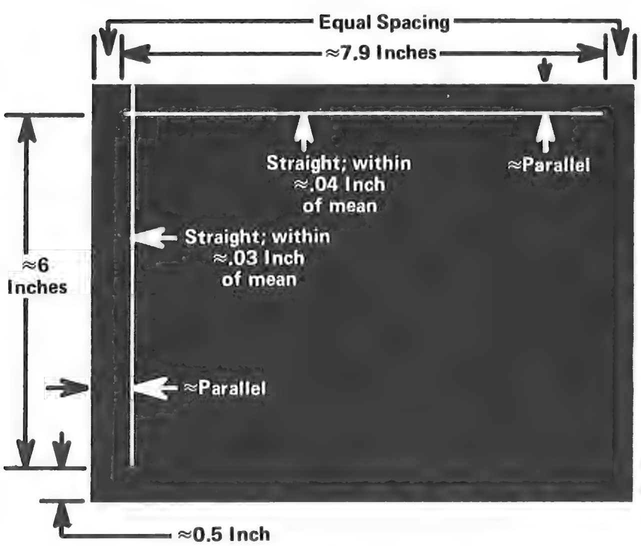


Fig. 4-8. Display Positioning, using Cross-hair Cursor.

e. If lines are excessively long, set X GAIN and/or Y GAIN fully counterclockwise. (These, and other display adjustments are located on the top of the Deflection Amp & Storage board in the display unit. See Fig. 4-6. Use Fig. 4-8 as a display reference.)

f. Adjust display positioning as follows:

(1) Adjust X POS for approximate left-right centering of horizontal line.

(2) Adjust Y POS to approximately center the vertical line segment described by its lower end and the point of intercept with the horizontal line (vertical thumbwheel at upper limit).

(3) If necessary, rotate the neck shield or yoke-mounting bracket (depending on assembly type) to obtain approximately equal spacing between the ends of the horizontal line and the top edge of the display area. Two nuts hold the yoke housing in place behind the center divider in the display unit (Fig. 4-6). Final adjustment and tightening of the yoke housing is done in a later step.

(4) Adjust X GEOM for approximate straightness of the vertical line; vertical line to be positioned as close to the left edge of the display area as possible by using the horizontal thumbwheel.

(5) Adjust Y GEOM for approximate straightness of the horizontal line, with the vertical thumbwheel at its upper limit.

(6) Adjust X GAIN for a horizontal line length of approximately 7.9 inches.

(7) Readjust X POS for approximate centering of the horizontal line.

(8) Adjust Y GAIN for approximately 6 inches between the bottom of the vertical line and the horizontal line intercept point. (Vertical potentiometer at upper limit.)

(9) Readjust Y POS to approximately center the area described in (8).

(10) Adjust X GEOM for optimum straightness of the vertical line.

(11) Adjust Y GEOM for optimum straightness of the horizontal line.

(12) Press PAGE and then enter four Zs. Check that the Zs are clearly noticeable as writing occurs. The Zs might or might not store at this time, depending on the position of the OP LEVEL adjustment. If the Zs are not clearly noticeable during writing, adjust R74, Character Brightness, on TC-1 (Fig. 4-7) and repeat the check.

(13) If the Zs do not store, gradually increase the OP LEVEL setting (Top of Deflection Amp & Storage board in display unit, Fig. 4-6) while entering Zs until they do store. Do not set OP LEVEL any higher than necessary.

(14) Press PAGE and again enter four Zs.

(15) Enter ESC and CTRL Z. The Zs should remain and the crosshair cursor should appear.

(16) Using the horizontal thumbwheel, place the vertical line so that it passes through a Z.

(17) Check vertical gain. The distance from the bottom of the vertical line to the top of a Z should be approximately 6.0 inches. If it is not, adjust Y GAIN to compensate for the error. (Adjust the bottom of the vertical line one-half of the desired total correction. An equal amount of correction will occur at the top of the line.) Then repeat steps (14), (15), and (17).

(18) Check vertical position. The bottom of the vertical line and the top of the Z should be equidistant from their respective horizontal edges of the display area. If not, adjust Y POS to center the display vertically. Observe the bottom of the vertical line during adjustment. Then repeat steps (14), (15), and (18).

(19) Recheck parallelism between the horizontal line and the top edge of the display area. Readjust the yoke housing rotation as necessary. (The yoke housing is held to the rear of the center wall in the display unit by two screws and nuts. The nuts must be loosened before the housing can be rotated.) Then tighten the yoke securing nuts.

(20) Recheck horizontal and vertical line straightness with lines positioned near the top and left edges, respectively. Readjust X GEOM for vertical line, and Y GEOM for horizontal line straightness as necessary.

(21) Position the cursor lines to various places on the display area and check for line straightness. If necessary, readjust X GEOM and Y GEOM for best overall compromise.

g. Press PAGE to return to Alpha Mode.

6. Storage Check/Adjustment (NORM COLL, OP LEVEL on Deflection Amp & Storage Board in display unit)

a. Remove the right side cover from the display unit, after removing its two screws. See Fig. 4-9.

b. Perform step 6b for adjusting a Terminal in which the CRT has not just been changed.

(1) Note the CE voltage value written on the tag attached to the top of the CRT shield in the display unit. Check for that value at pin 3 on J55 (Fig. 4-9), with the Terminal in View status. (Press SHIFT to regain View status.)

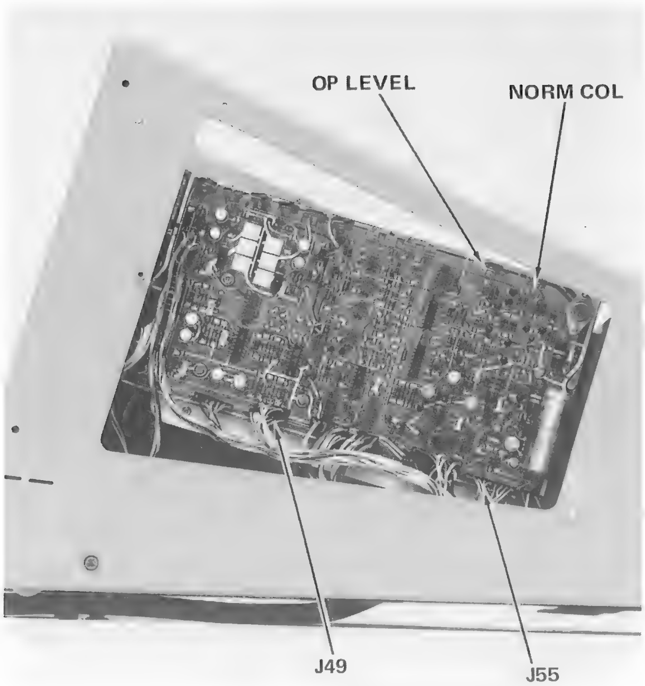


Fig. 4-9. High Voltage and Z Axis board.

(2) Adjust NORM COLL (top of Deflection Amp & Storage board in the display unit, Fig. 4-9) to obtain the specified value at pin 3.

(3) Note the STORAGE LEVEL value written on the tag attached to the top of the CRT shield. Check for that value at pin 4 on J55 (Fig. 4-9).

(4) Adjust OP LEVEL (Fig. 4-9) to obtain the specified value.

(5) Put the LOCAL/LINE switch at LINE. Then go to step 6d.

c. Perform step 6c for adjusting a Terminal in which the CRT has just been changed.

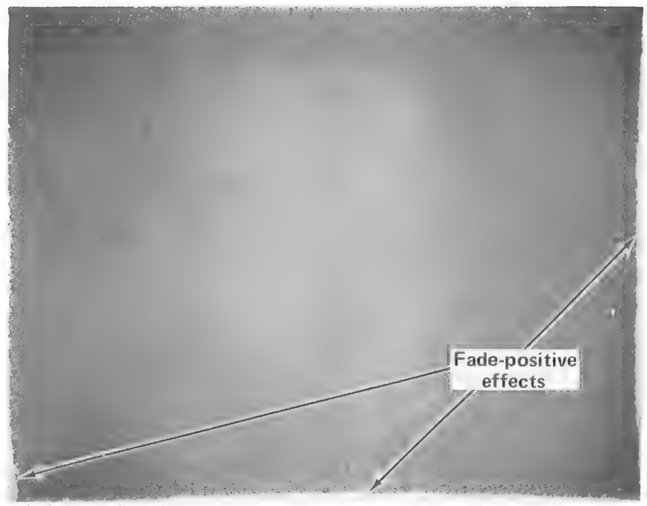
(1) Note the CE Voltage value written on the tag supplied with the replacement CRT. Adjust NORM COLL to obtain that CE Voltage at pin 3 on J55. See Fig. 4-9.

(2) Connect the voltmeter to pin 4 of J55 on the Deflection Amp & Storage board (Fig. 4-9), expecting approximately +200 V DC.

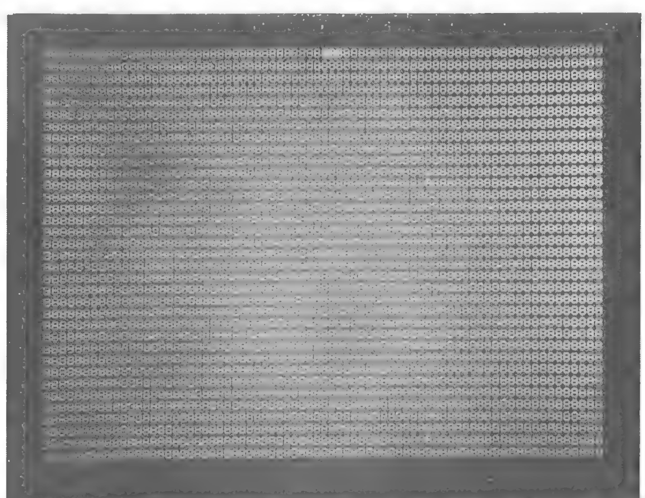
(3) Set OP LEVEL fully counterclockwise. Then adjust it clockwise in moderate increments, pressing PAGE between increments, until a point is reached where the edges of the display area start to become obviously brighter, or "fade positive" right after an erase cycle. (See Fig. 4-10A). Record the voltage which exists on pin 4 of J55.

(4) Reduce the OP LEVEL setting slightly, just to the point where fade positive no longer occurs after PAGE is pressed.

(5) Put the LOCAL/LINE switch at LINE and press the 8 key. The display should fill with 8s.



(A) Fade-Positive



(B) Drop-Out

Fig. 4-10. Display Conditions.

(6) Turn the OP LEVEL counterclockwise until the displayed numbers appear to degrade due to dots disappearing (dropping out). See Fig. 4-10B. Record the J55 pin 4 voltage at which this occurs. (Press the SHIFT key as necessary to maintain View status.)

(7) Determine the mid-voltage between the two recorded voltages. Set the OP LEVEL to obtain this value at pin 4.

d. Press PAGE and then press 8. The display should become filled with 8s. Wait approximately five minutes and view the display, checking for drop-out or fade-positive conditions. If drop-out occurs, adjust the OP LEVEL in five-volt positive increments and repeat the check. If fade-positive occurs, adjust in five-volt negative increments and repeat the check. (If both conditions occur, the CRT is near the end of its useful life, and a slight fade-positive condition must be tolerated if drop-out is to be avoided.)

e. Upon completion of step d, measure the voltage at pin 4 on J55 and write the value opposite STORAGE LEVEL on the tag on the CRT shield.

f. Observe the overall brightness uniformity of the screen. This is controlled to a great extent by the CE voltage (NORM COLL adjustment), and affects uniformity of storing, drop-out, focus, and hard copy. If the overall screen brightness appears too uneven, NORM COLL can be experimented with to achieve better results. Perform the following:

(1) Connect the voltmeter to J55, pin 3 on the Deflection Amp & Storage board (Fig. 4-9), expecting about +100 V.

(2) Press PAGE and 8 to renew the display.

(3) Adjust NORM COLL in small increments pressing PAGE and 8 after each adjustment. Note the voltage at pin 3 and the effect on display uniformity.

(4) Select the position which provides the brightest display consistent with optimum uniformity and record the voltage. The best position usually occurs at a voltage slightly more positive than that which provides maximum display brightness. A too-positive voltage will often cause obvious streaking or shadows around some characters. A too-negative voltage may result in oscillation which causes the screen to appear to blink rapidly. A too-negative voltage may also give a mottled effect to some of the stored characters.

(5) Record the selected NORM COLL voltage on the tag attached to the CRT shield. If the CRT has not been replaced, do not obliterate the old voltage value; simply draw a line through it and write the new value alongside. The new voltage normally will not differ greatly from the old one. In the case of a replacement CRT, obliterate the old value and write in the new one. The new voltage normally will not differ greatly from that supplied with the CRT.

7. Writing Intensity Check/Adjustment (R86, Writing Intensity on High Voltage & Z Axis Board on display unit)

a. Turn the Terminal off.

b. On the Interface card in the pedestal, remove the jumper which connects $\overline{\text{T STROBE}}$ to $\overline{\text{C STROBE}}$. (The jumper is either on an Extender Card or on an Integrated Circuit Test Clip.)

c. Check the position of the FUZZ strap on the High Voltage & Z Axis board in the display unit. (Fig. 4-11.) The strap should always be in the position shown.

d. Turn the Terminal on.

e. Put the LOCAL/LINE switch at LOCAL.

f. Press PAGE to erase the display.

g. While observing the Alpha cursor, adjust R86, Writing Intensity (on the High Voltage & Z Axis board, Fig. 4-11) until the Alpha cursor intensity diminishes to where it can barely be seen.

h. Press PAGE to erase the display.

i. Enter CTRL SHIFT M at the keyboard to put the Terminal in Graph Mode.

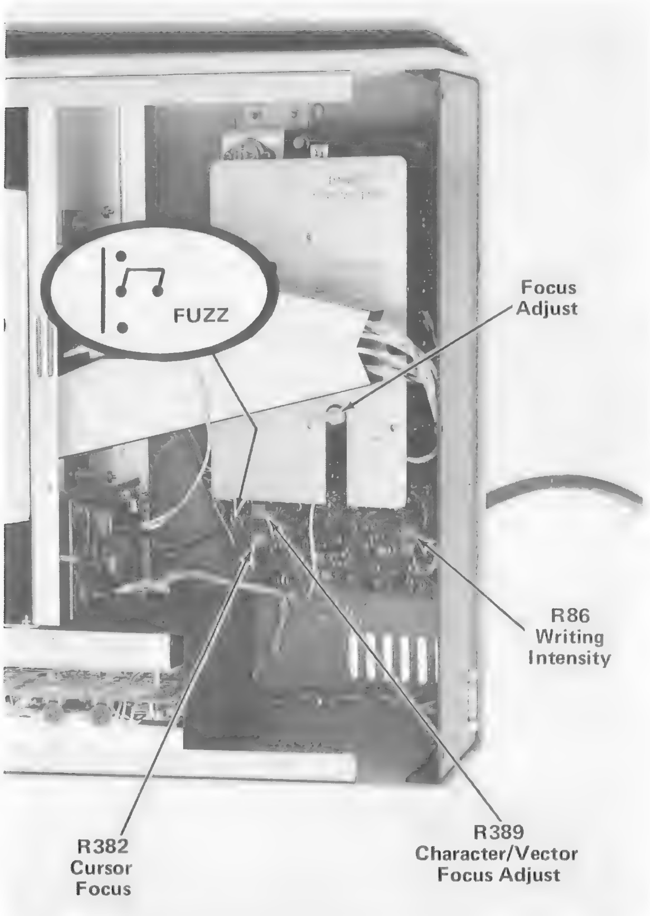


Fig. 4-11. Adjustments and Test Point locations.

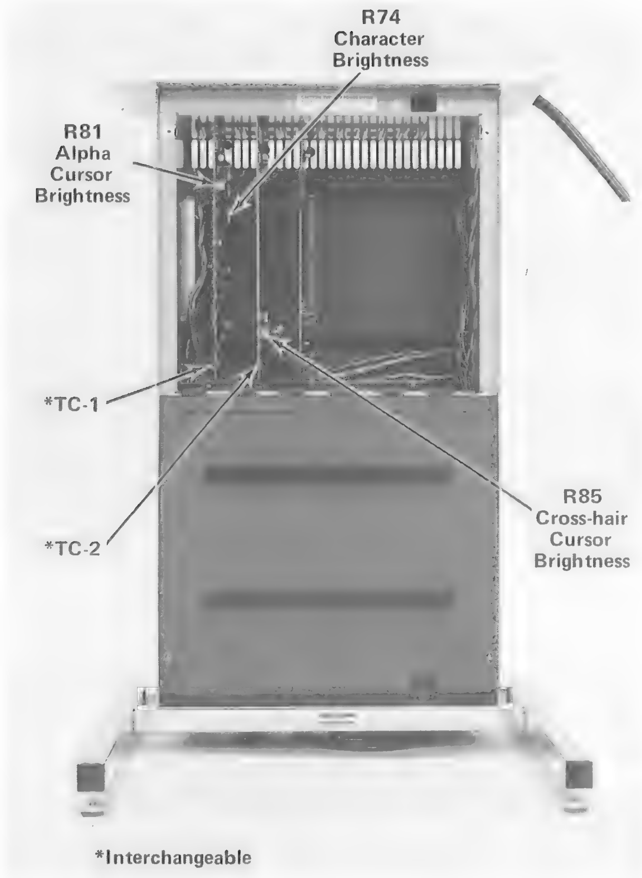


Fig. 4-12. Adjustment locations in pedestal.

j. Enter the following characters to draw a vector from the bottom-left of the display to the top-right.

Space\` Space @ 8 k ? _

k. Check vector writing. A vector should have been drawn from the bottom-left corner to the top-right corner of the display. Some or all of it may be missing. If a complete vector is drawn from the bottom-left to the top-right corner, press PAGE and again adjust R86 to diminish the intensity of the Alpha cursor. It may be necessary to increase the setting of R81, Alpha Cursor Brightness, on edge of TC-1 (Fig. 4-12), to keep a visible cursor so the effect of the R86 adjustment can be observed.

l. Repeat steps h through k until a partial vector is obtained.

m. Press PAGE and then adjust R86 about 10 degrees to increase the intensity of the Alpha cursor slightly.

n. Enter CTRL SHIFT M Space\` Space @ 8 k ? _ and check for a complete vector, drawn from the bottom-left to the top-right. If the vector remains broken, repeat steps m and n until it is satisfactory.

o. Enter PAGE and CTRL SHIFT M and Space\` Space @ 8 k ? _ 8 k Space @ Space\` ? _ 8 k ? _ and check for complete vectors. If incomplete or insufficiently bright, repeat steps m and o.

p. Enter PAGE and CTRL SHIFT M and 8 k Space @ Space\` Space @ Space\` ? _8 k Space @ 8 k ?_ and check for complete vectors. If incomplete or insufficiently bright, repeat steps m and p.

NOTE

Tube life varies inversely with intensity. Therefore, the intensity should always be adjusted for minimum brightness consistent with good viewing of complete vectors.

8. Alpha Cursor Brightness Check/Adjustment (R81, Alpha Cursor Brightness on TC-1 in the pedestal)

a. Press PAGE to erase the display.

b. Note the intensity of the Alpha cursor. It should be bright enough for convenient viewing, but not so bright that it stores.

c. Adjust Alpha Cursor Brightness (R81 on edge of TC-1) to obtain the desired intensity. See Fig. 4-12 for adjustment location. If the cursor continues to store with R81 at minimum intensity, the R86 Writing Intensity adjustment may be set too high; step 7 should be re-checked.

9. Alpha Character Brightness Check/Adjustment (R74, Character Brightness on TC-1 in the pedestal)

a. Enter several writing characters and note the writing brightness.

b. Adjust Character Brightness (R74 on TC-1, Fig. 4-12) for desired brightness, entering additional characters to check results. Adjustment will not affect previously-stored characters.

c. Enter PAGE and CTRL SHIFT M and then enter the following to draw a vector:

```
, f ` _ f 8 @
```

d. Enter RESET while holding down the SHIFT key, to enter Alpha Mode without erasing.

e. Using the LF and Space keys, place the cursor near the left end of the vector, either above or below it.

f. Enter writing characters and compare the character and vector brightness. If necessary, adjust the character brightness to provide characters whose intensity is comparable to the vector brightness.

g. Press PAGE to erase the display.

10. Character and Vector Focus Check/Adjustment (FOCUS ADJUST and R389, Character/Vector Focus Adjust on High Voltage & Z Axis board in display unit)

a. Press PAGE.

b. Enter an e character and check its focus.

c. Adjust FOCUS ADJUST (alongside yoke housing in display unit — Fig. 4-11) in small increments, entering e after each adjustment, until optimum appearance is achieved. Press PAGE as necessary to keep the writing in the corner of the display.

d. Turn the Terminal off.

e. Reconnect the $\overline{\text{CSTROBE}}$ to $\overline{\text{TSTROBE}}$ strap which was removed in step 7b.

f. Turn the Terminal on.

g. Switch the LOCAL/LINE switch to LINE. Press e and the display should fill up. Compare the writing in the four corners. (Ignore other areas of the display.) It should appear similar. If noticeable difference exists, slightly adjust FOCUS ADJUST. Press PAGE and then recheck. Repeat until the best focus compromise is achieved for the four corners.

h. Note the focus of the characters near the center of the display. It is desirable that they be similar to the focus achieved in the corners. To adjust, proceed as follows:

(1) Place the LOCAL/LINE switch at LOCAL.

(2) Press PAGE.

(3) Using the Space Bar, LF, RETURN, and e keys, enter several e characters in each of the four corners. Then position the cursor to the center of the display area.

(4) Alternately enter the e character and adjust R389 — Character/Vector Focus (on High Voltage & Z Axis board in the display unit, Fig. 4-11) until center focus and corner focus are approximately the same.

i. Place the LOCAL/LINE switch at LINE. Then press PAGE.

j. Enter an 8 and the display should fill with 8s.

k. Check the display. The overall display should have approximately even focus. If unsatisfactory, repeat steps e through h one time to provide optimum overall focus. Note that character brightness affects the writing of characters, and may have to be increased or decreased to provide a good compromise between brightness and focus. As previously noted, the NORM COLL adjustment also affects focus. If all else fails, it can be experimented with. However, after readjusting it, this procedure must be resumed at step 7.

11. Crosshair Cursor Intensity Check/Adjustment [R29, Crosshair Cursor Brightness on TC-2 (R85 on Boards Numbered 670-1729-04 and Below)]

a. Put the LOCAL/LINE switch at LOCAL.

b. Set the cursor thumbwheels near midrange.

c. Press PAGE. Then enter ESC and CTRL Z to obtain a crosshair cursor.

d. If necessary, adjust R29 (R85 on boards numbered 670-1729-04 and below) — Crosshair Intensity (on TC-2, Fig. 4-12) so that the cursor can be seen.

e. Move the thumbwheels and check to see if the cursor stores. Readjust R29 (R85 on boards numbered 670-1729-04 and below) as necessary to provide a clearly visible non-storing cursor.

12. Cursor Focus Check/Adjustment (R382, Cursor Focus on High Voltage & Z Axis Board in display unit)

a. Place the intersect point at mid-screen, using the thumbwheels.

b. Adjust Cursor Focus (R382 on the High Voltage & Z Axis board in the display unit, Fig. 4-10) for uniform focus of the lines.

c. Move the cursor to various positions on the screen. If necessary, adjust R382 to obtain the most uniform line focusing throughout the display.

d. Press PAGE to return to Alpha Mode.

13. Vector Drawing Time Check

a. Turn the Terminal off.

b. Remove the $\overline{\text{T STROBE}}$ to $\overline{\text{C STROBE}}$ strap from the Extender Card or Integrated Circuit Test clip.

c. Turn the Terminal on.

d. Connect the oscilloscope probe to J49 pin 1 on the Deflection Amp & Storage board (Fig. 4-9). Set the oscilloscope sensitivity to 2 V/division and the sweep rate to 1 ms/division.

e. Press PAGE. Then enter CTRL SHIFT M.

f. Enter the following: ? RUBOUT ? _.

g. Repeatedly press _ while checking the oscilloscope waveform. (The _ will repeatedly execute an off-screen vector.)

h. Check the duration of the negative-going waveform on the oscilloscope. It should be approximately 2.6 ms, and is an indication of the vector drawing time. (It is non-adjustable, and is a function of a count-down circuit on TC-1.)

14. Vector Dynamic Geometry Error Check

a. Press PAGE. Then enter CTRL SHIFT M.

b. Enter Space` Space @ to set the beam to 0, 0.

c. Enter 8 k 8 K to draw a vector from 0, 0 to 779, 779.

d. Enter Space` Space @ to draw a vector from 779, 779 to 0, 0.

e. Check that the separation between the two lines does not exceed 3% of the total line length (approximately 0.25 inch) at any point. See Fig. 4-13.

f. Press PAGE to erase the display.

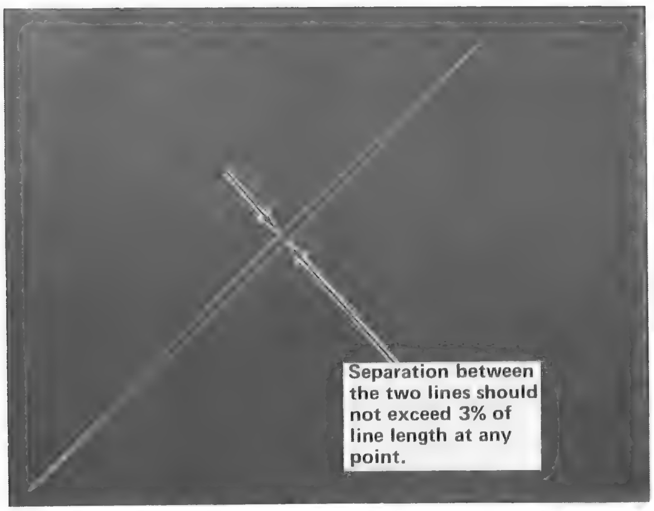


Fig. 4-13. Vector dynamic geometry illustration.

15. Vector Parallelism Check

a. Enter PAGE and CTRL SHIFT M.

b. Enter the following sequence to draw a rectangle:

Space` Space @ 8 k @ k ? _ Space ` _ ` Space @

c. Measure and record the length of all lines.

d. Check parallelism. The difference in the length of the horizontal lines should not exceed 2% of the vertical line length. The difference in the length of the vertical lines should not exceed 2% of the horizontal line length. With the Terminal adjusted as outlined in this procedure, the line length is approximately 7.9 inches horizontal and 6 inches vertical. Line length difference should not exceed approximately 0.16 inch horizontal and approximately 0.12 inch vertical.

16. Character Transmission and Writing Check

a. Check that each ASCII writing character appears on the screen in response to key entry.

b. Activate the TTY LOCK by pressing the key. The key should remain down or become lighted, depending on the type of keyboard.

c. Press each writing character key and note character writing is limited to the TTY code. The TTY LOCK function key affects the code being transmitted.

d. Release the TTY LOCK key by pressing it once.

17. Control Character Transmission and Response Check

a. With the LOCAL/LINE switch at LOCAL, enter the following at the keyboard and check the response:

CONTROL CHARACTER RESPONSE CHECK

Command	Code Equivalent	Response
CTRL SHIFT K and CTRL L	ESC FF	Erases display, homes cursor
CTRL G	BEL	Rings Bell
CTRL I	HT	Moves cursor one space to right
CTRL H	BS	Moves cursor back one space
CTRL J	LF	Moves cursor down one line; if LF EFFECT strap is at LF→CR, the cursor will also move to the left margin.

CONTROL CHARACTER RESPONSE CHECK (cont)

Command	Code Equivalent	Response
CTRL K	VT	Moves cursor up one line
CTRL SHIFT M	GS	Selects Graph Mode and dark vector
Space RUBOUT Space _	SP DEL SP _	Executes a dark vector and sets the Terminal for a bright vector
Ø @	Ø @	Draws a vector
CTRL SHIFT M	GS	Sets the Terminal for a dark vector
Λ	Λ	Executes a dark vector and sets the Terminal for a bright vector
Λ	Λ	Writes a point
CTRL SHIFT O	US	Switches back to Alpha without moving the writing beam
CTRL SHIFT M	GS	Selects Graph Mode
Λ	Λ	Executes a dark vector and resets for a bright vector
2 x & H	2 x & H	Draws a vector
CTRL M	CR	Switches to Alpha Mode and moves writing beam to margin Ø; if CR EFFECT option is at CR→LF, a line feed will also occur
CTRL SHIFT K and CTRL Z	ESC SUB	Selects GIN Mode and displays the crosshair cursor
Put LOCAL/LINE switch at LINE; then enter Space	SP	Crosshair cursor disappears and the Alpha cursor reappears

b. Press PAGE and place the LOCAL/LINE switch at LOCAL.

18. Hard Copy Amplitude and Position Check/Adjustment (HC X AMP, HC Y AMP, FAST RAMP POS, SLOW RAMP POS on the Deflection Amp & Storage Board in display unit)

a. Turn the Terminal off.

b. Replace the $\overline{\text{T STROBE}}$ to $\overline{\text{C STROBE}}$ strap which was removed in step 13.

c. Turn the Terminal on.

d. At the Hard Copy Unit, remove the copying paper (or disable the paper drive) to avoid waste during this procedure. If necessary, refer to the Hard Copy Unit manual for instructions.

e. Connect the Hard Copy Unit to the Terminal, via the Hard Copy connector (J525) on the back of the display unit.

f. Set the HC X AMP potentiometer (top of Deflection Amp & Storage board in the display unit, Fig. 4-14) fully clockwise.

g. Turn the Hard Copy Intensity on the side of the display unit (Fig. 4-14) fully clockwise.

h. Press the MAKE COPY button and note that a scan bar moves up the screen. If the scan bar does not appear and store as in Fig. 4-15, adjust R91, Coarse Hard Copy Intensity (on the High Voltage & Z Axis board in the display unit, Fig. 4-14) until the bar does store. Press PAGE and MAKE COPY between adjustments.

i. Set the LOCAL/LINE switch to LINE. Press PAGE and 8 to write a page full of 8s.

j. Press MAKE COPY. The Hard Copy scan bar should store on the display area, but should be narrower than the stored 8s, similar to Fig. 4-15A. (If the scan bar is wider than the stored 8 display, the HC X AMP potentiometer may be set to the wrong limit.)

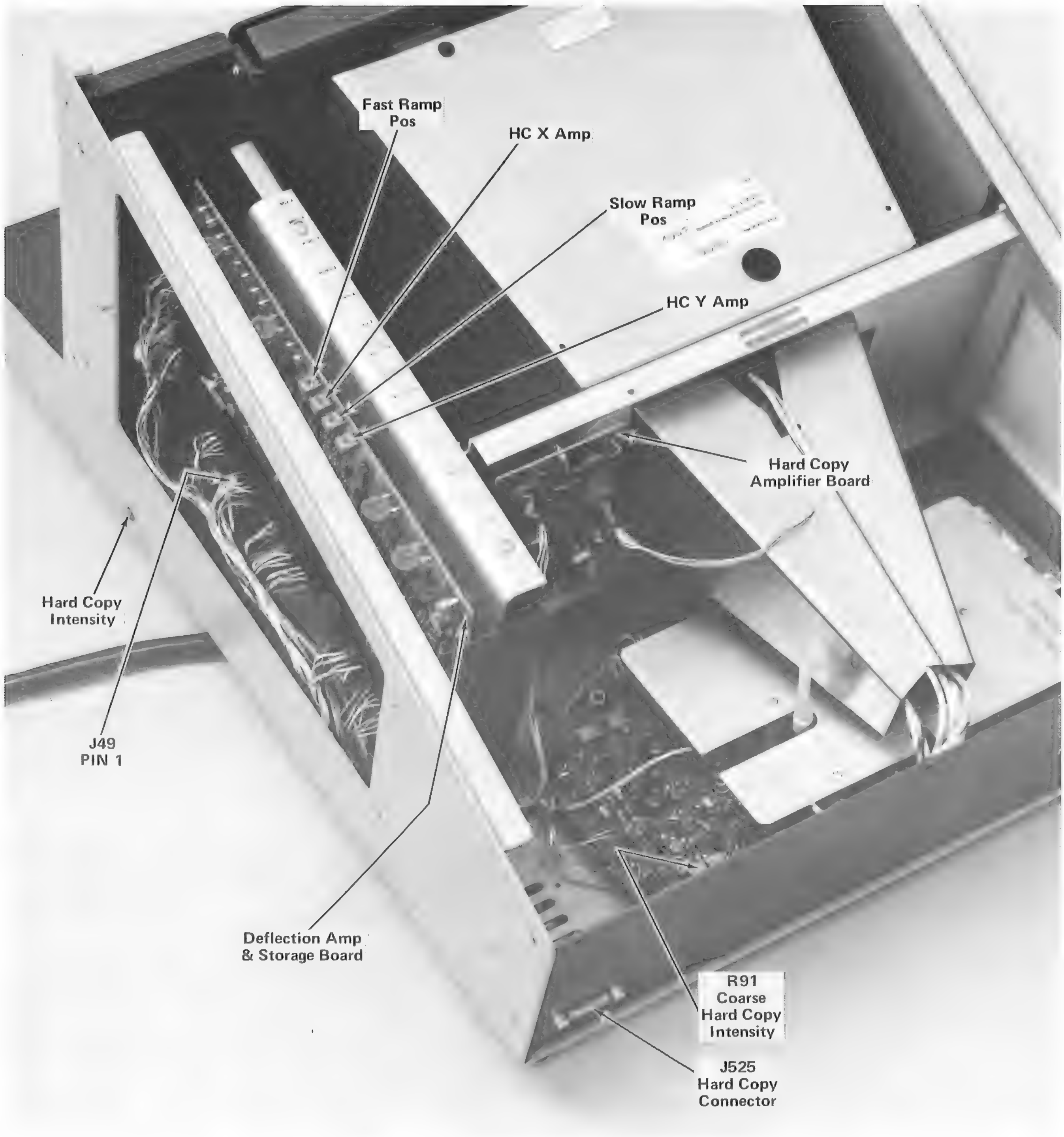


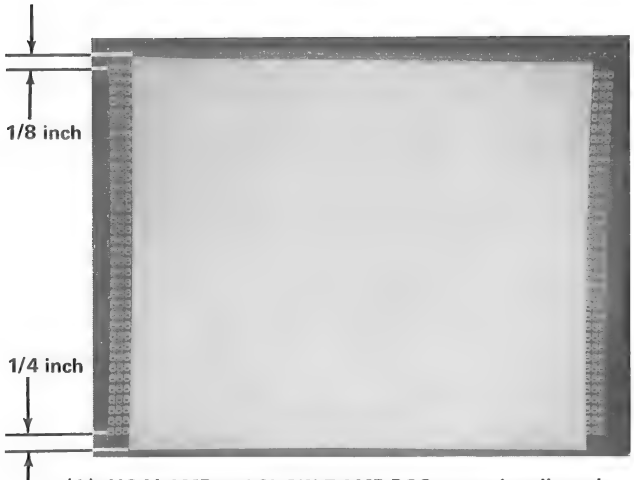
Fig. 4-14. Hard Copy adjustment and test point locations.

k. Check Hard Copy Y amplitude. The stored scan bar should extend approximately 1/4 inch below and 1/8 inch above the stored 8s, as in Fig. 4-15A.

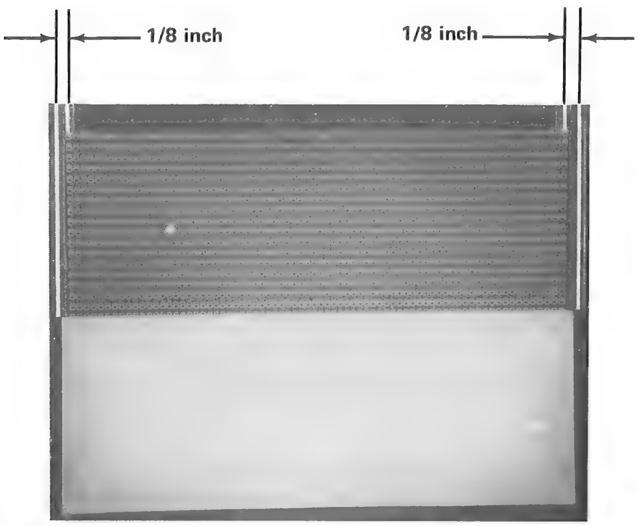
l. Adjust HC Y AMP and the SLOW RAMP POS (on the Deflection Amp & Storage board) in small increments, repeating steps j, k, and l until results listed in step k are obtained.

m. Press PAGE and 8 to refill the page.

n. Insert the screwdriver in the FAST RAMP POS potentiometer slot. Then press MAKE COPY and adjust the



(A) HC Y AMP and SLOW RAMP POS properly adjusted.



(B) HC X AMP and FAST RAMP POS properly adjusted.

Fig. 4-15. Hard Copy amplitude and position adjustment displays.

FAST RAMP POS as the scan bar sweeps up the screen, striving to center the scan bar on the display as in Fig. 4-15(A). Repeat steps m and n as necessary.

o. Insert the screwdriver in the HC X AMP potentiometer on the Deflection Amp & Storage board. Then press MAKE COPY and adjust the HC X AMP as the bar scans the display area, until the bar extends approximately 1/8 inch beyond each side as in Fig. 4-15(B). Press PAGE and 8 and MAKE COPY if necessary to refill the screen to complete the adjustment. Readjust the FAST RAMP POS (step n) if refinement of the centering is necessary.

19. Hard Copy Intensity Adjustment (R91, Coarse Hard Copy Intensity on the High Voltage & Z Axis Board in the display unit, and the Hard Copy Intensity on the side of the display unit)

a. Press PAGE and MAKE COPY. Set Hard Copy Intensity (side of display unit) to mid-position. Then adjust R91, Coarse Hard Copy Intensity (on High Voltage & Z Axis board inside display unit, Fig. 4-14) to a point just below that at which the scan bar does any storing. Repeat as necessary to eliminate storing at all points on the display area.

20. Hard Copy Threshold Check/Adjustment (R167, Hard Copy Threshold on Hard Copy Amplifier Board in display unit)

a. Set the oscilloscope for alternate trace operation. Set each vertical channel for 0.5 V/division. Neither channel should be inverted. Set the sweep rate to 0.5 μs/division. Set both input switches to ground and set both traces to the second horizontal graticule line from the bottom. Then switch both input switches to DC.

b. Connect a probe from the oscilloscope's external trigger jack to the Z signal line at J49 Pin 1 on the Deflection Amp & Storage board in the display unit (Fig. 4-14). Switch the oscilloscope to external triggering.

c. Connect a probe from channel 1 of the oscilloscope to TP85 on the Hard Copy Amplifier board (Fig. 4-16). Connect the probe ground lead to the ground test point on the board.

d. Connect a probe from channel 2 of the oscilloscope to TP195 on the Hard Copy Amplifier board (Fig. 4-16). Connect the probe ground lead to ground on the board.

e. Press PAGE and then press MAKE COPY and check for an oscilloscope display as in Fig. 4-17. The peaks of the most prominent pulses should almost touch.

f. Adjust R167—Hard Copy Threshold (on the Hard Copy Amplifier board, Fig. 4-16) until the peaks almost touch as in Fig. 4-17. The separation may vary with the vertical position of the scan bar on the screen. If so, adjust for minimum separation of the closest pulses.

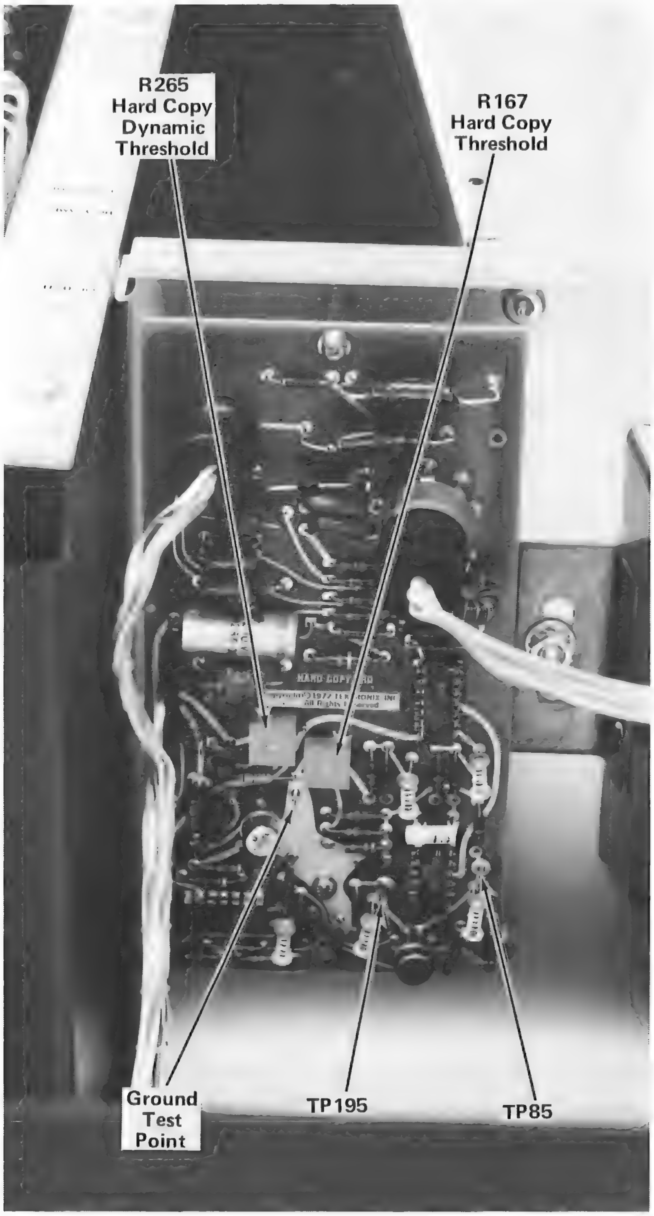


Fig. 4-16. Hard Copy threshold adjustment and test point locations. Location within the display unit is shown in Fig. 4-14.

21. Hard Copy Dynamic Threshold Check/ Adjustment (R265, Dynamic Threshold Adjust on Hard Copy Amplifier Board)

a. Switch the oscilloscope sweep rate to 1 ms/division.

b. Press MAKE COPY and check for a display as in Fig. 4-18(B). The vertical separation between the pulse peaks of the two traces should remain fairly constant as the hard copy bar scans.

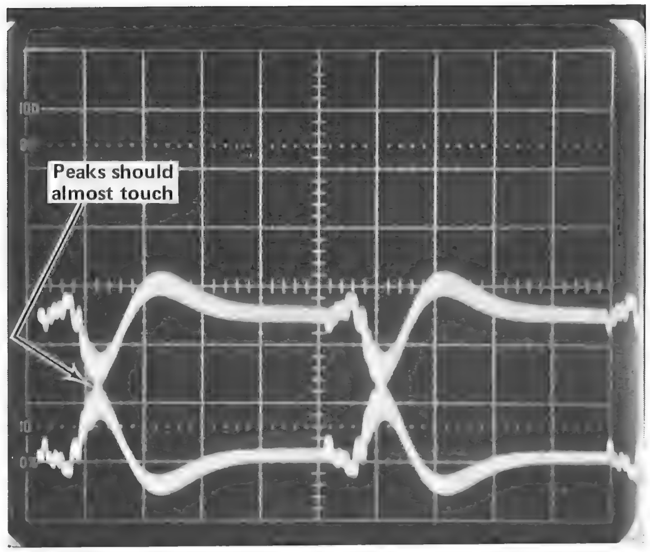


Fig. 4-17. Hard Copy Threshold adjustment waveform. 0.5 V/ division vertical; 0.5 μs/division horizontal.

c. Press MAKE COPY and adjust R265, Dynamic Threshold Adjust (Fig. 4-16) until the separation between the pulse peaks remains fairly constant as the Hard Copy bar scans. The appearance may change with the vertical position of the scan bar; in that case, adjust for the best compromise.

d. If the Dynamic Threshold was grossly out of adjustment, steps 19 and 20 should be repeated.

22. Hard Copy Writing Check

a. Re-install the paper in the Hard Copy Unit or engage the paper drive, as appropriate.

b. Press PAGE. Then press the A key to write a full page on the display unit.

c. Press MAKE COPY. The Hard Copy Unit should make a copy of the display.

d. Examine the copy for writing quality. Assuming that the Hard Copy Unit is properly adjusted, writing quality is controlled by the following adjustments in the Terminal:

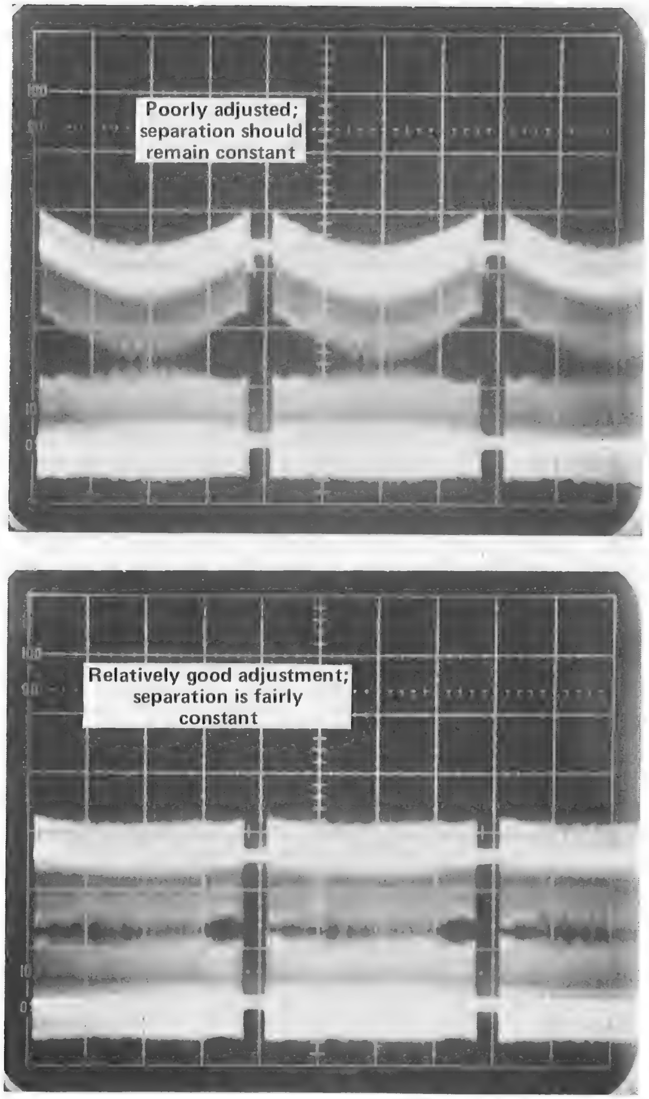


Fig. 4-18. Hard Copy Dynamic Threshold adjustment waveform. 0.5 V/division vertical; 1 ms/division horizontal.

Condition	Possible Causes
Information does not copy or information drop-out occurs	Mis-adjusted Hard Copy Intensity setting on side of display unit (step 19); Scanning pulses too far apart (step 20); Pulse separation not constant (step 21).
Excessive background writing (noise)	Hard Copy Intensity setting on side of display unit set too high (step 19); Insufficient separation between scanning pulses (step 20).
Information missing around perimeter	Underscan caused by HC X AMP and/or HC Y AMP (top-left in pedestal) being set too low (step 18).
Information missing from one vertical edge	SLOW RAMP POS not properly set (step 18).
Information missing from one horizontal edge	FAST RAMP POS not properly set (step 18)
Copy too small; bars on edge or edges of paper	HC X AMP and/or HC Y AMP set too high (step 18). FAST RAMP POS or SLOW RAMP POS improperly set (step 18).

NOTE

If the copying information in the various areas of the copy is unacceptable, and all else fails, the NORM COLL voltage may have to be adjusted to provide satisfactory results. However, the NORM COLL adjustment also affects uniformity of storing, dropout, focus, and intensity. If readjusted, steps 7 through 12 and step 22 should be repeated.

e. If the copy appears satisfactory, make five copies of the same full page display. The fifth copy should remain satisfactory, with minimum degradation due to repetitive scanning of the displayed data. If the fifth copy is unacceptable, decrease the Hard Copy Intensity setting slightly and repeat step e.

f. Disconnect the probes from the display unit.

23. Restoring Original Conditions

a. Turn the Terminal OFF and disconnect the line plug from the power source.

b. Remove the pedestal cover, if it had been replaced in step 2.

c. If necessary, remove the transformer protection plate and the line fuse and rewire the Terminal transformer to its previous configuration. Then replace the transformer protection plate.

d. Reset the option straps on TC-1 and the Interface Card to the condition recorded in the Preliminary Procedure.

e. Remove the Extender Card or Integrated Circuit Test Clip(s). Remove the jumper strap(s) which was installed in the Preliminary Procedure. (Data Communication Interface 021-0065-00 on J360; TTY Port Interface on J161 and J162.)

f. Reconnect the output cable to the Interface Card if a Data Communication Interface 021-0065-00 or a TTY Port Interface is installed; reset the rear panel switches to their previous positions if an Optional Data Communication Interface 021-0074-00 is in use.

g. Install any accessory cards which are to be used with the Terminal. If desired, check them out, referring to their documentation.

h. Check that the proper fuse is installed in the pedestal cover (2 A slow blow for 115 V, 1.25 A slow blow for 230 V) and then replace the cover.

i. Re-install the side cover and top cover on the display unit.

j. If desired, install the display unit on the pedestal unit, following the procedure given in Section 1.

ELECTRICAL PARTS LIST

Replacement parts should be ordered from the Tektronix Field Office or Representative in your area. Changes to Tektronix products give you the benefit of improved circuits and components. Please include the instrument type number and serial number with each order for parts or service.

ABBREVIATIONS AND REFERENCE DESIGNATORS

A	Assembly, separable or repairable	FL	Filter	PTM	paper or plastic, tubular molded
AT	Attenuator, fixed or variable	H	Heat dissipating device (heat sink, etc.)	R	Resistor, fixed or variable
B	Motor	HR	Heater	RT	Thermistor
BT	Battery	J	Connector, stationary portion	S	Switch
C	Capacitor, fixed or variable	K	Relay	T	Transformer
Cer	Ceramic	L	Inductor, fixed or variable	TP	Test point
CR	Diode, signal or rectifier	LR	Inductor/resistor combination	U	Assembly, inseparable or non-repairable
CRT	cathode-ray tube	M	Meter	V	Electron tube
DL	Delay line	Q	Transistor or silicon-controlled rectifier	Var	Variable
DS	Indicating device (lamp)	P	Connector, movable portion	VR	Voltage regulator (zener diode, etc.)
Elect.	Electrolytic	PMC	Paper, metal cased	WW	wire-wound
EMC	electrolytic, metal cased	PT	paper, tubular	Y	Crystal
EMT	electrolytic, metal tubular				
F	Fuse				

Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Description
		DISPLAY UNIT CHASSIS		
DIODES				
CR1090	150-1001-00			LIGHT EMMITING DIODE,2V,70MA
CR1092	150-1001-00			LIGHT EMMITING DIDOE,2V,70MA
BULB				
DS1000	150-0134-00			INCANDESCENT,6.3V,200MA,GREEN LENS
INDUCTOR				
L1000A,B	119-0422-00			YOKE,CRT ASSEMBLY
RESISTORS				
R1050	311-0642-00			20K OHM,VAR
R1070	311-0546-00			10K OHM,VAR
R1072	311-0546-00			10K OHM,VAR
R1076	311-1044-00			50K OHM,VAR
SWITCHES				
S1001	260-1179-01			ROCKER,TOGGLE,DPST,POWER
S1080	260-1334-00			ROCKER,SLIDE,SPDT,SW1
S1081	260-1334-00			ROCKER,SLIDE,SPDT,SW2
S1082	260-1334-00			ROCKER,SLIDE,SPDT,SW3
S1083	260-1334-00			ROCKER,SLIDE,SPDT,SW4
S1085	260-1274-00			ROCKER,SPDT,MAKE COPY
S1087	260-1334-00			ROCKER,SLIDE,SPDT,LOCAL
SPEAKER				
SP1000	119-0305-00			LOUDSPEAKER,PERMANENT MAGNET,45 OHM,2W
ELECTRON TUBE				
V1	154-0690-00			CRT

Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Description
		PEDESTAL CHASSIS		
CAPACITORS				
C41	290-0422-01			5400UF,ELECT.,15V,+75-10%
C501	283-0022-00			0.02UF,CER,900V/1400V
C502	283-0022-00			0.02UF,CER,900V/1400V
DIODES,SILICON				
CR502	152-0274-00			RECTIFIER,100V,12A,SELECTED FROM 1N1200
CR503	152-0274-00			RECTIFIER,100V,12A,SELECTED FROM 1N1200
FUSES				
F501	159-0023-00			CARTRIDGE,2A,3AG,SLO-BLO(115V)
F501	159-0041-00			CARTRIDGE,1A,3AG,SLO-BLO(230V)
TRANSISTORS				
Q510	151-0337-00			SILICON,NPN,2N3055
Q515	151-0337-00			SILICON,NPN,2N3055
Q520	151-0337-00			SILICON,NPN,2N3055
RESISTOR				
R501	302-0104-00			100K OHM,0.50W,10%
TRANSFORMER				
T501	120-0768-01			POWER
		A1 ASSEMBLY TC-1		
ASSEMBLIES				
A1	670-2372-00	B010100	B010131	CIRCUIT CARD ASSEMBLY, TC-1
A1	670-2372-01	B010132		CIRCUIT CARD ASSEMBLY, TC-1
A1	670-2372-02			CIRCUIT CARD ASSEMBLY, TC-1
CAPACITORS				
C13	290-0530-00			68UF,ELECT.,6V,20%
C32	290-0536-00			10UF,ELECT.,25V,20%
C54	283-0602-00			53PF,MICA,300V,5%
C58	281-0546-00			330PF,CER,500V,10%
C101	283-0003-00			0.01UF,CER,150V,+80-20%
C142	283-0003-00			0.01UF,CER,150V,+80-20%
C146	283-0602-00			53PF,MICA,300V,5%
C161	283-0003-00			0.01UF,150V,+80-20%
C235	281-0546-00			330PF,CER,500V,10%
C279	281-0551-00			390PF,CER,500V,10%
C382	290-0529-00			47UF,ELECT.,20V,20%
C396	283-0003-00			0.01UF,CER,150V,+80-20%
C443	290-0530-00			68UF,ELECT.,6V,20%
C444	283-0003-00			0.01UF,CER,150V,+80-20%
C509	283-0003-00			0.01UF,CER,150V,+80-20%
C546	283-0065-00			0.001UF,CER,100V,5%

TC-1 (cont)

Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Description
CAPACITORS (cont)				
C565	290-0529-00			47UF,ELECT.,20V,20%
C575	290-0529-00			47UF,ELECT.,20V,20%
DIODES,SILICON				
CR452	152-0141-02			1N4152
CR546[1]	152-0141-02			1N4152
CR553	152-0141-02			1N4152
TRANSISTORS				
Q32	151-0302-00			SILICON,NPN,2N2222A
Q81	151-0190-02			SILICON,NPN,2N3904
Q385	151-0302-00			SILICON,NPN,2N2222A
Q432	151-0302-00			SILICON,NPN,2N2222A
Q438	151-0192-00			SILICON,NPN,SELECTED FROM MPS6521
RESISTORS				
R13	315-0223-00			22K OHM,0.25W,5%
R14	315-0472-00			4.7K OHM,0.25W,5%
R15	315-0472-00			4.7K OHM,0.25W,5%
R16[1]	315-0472-00			4.7K OHM,0.25W,5%
R31	315-0103-00			10K OHM,0.25W,5%
R45	321-0147-00			332 OHM,0.125W,1%
R46	315-0681-00			680 OHM,0.25W,5%
R55	321-0177-00			681 OHM,0.125W,1%
R56	321-0147-00			332 OHM,0.125W,1%
R57	315-0101-00			100 OHM,0.25W,5%
R74	311-1285-00			25K OHM,VAR
R75	315-0472-00			4.7K OHM,0.25W,5%
R76	315-0472-00			4.7K OHM,0.25W,5%
R77	315-0202-00			2K OHM,0.25W,5%
R78	315-0152-00			1.5K OHM,0.25W,5%
R81	311-1285-00			25K OHM,VAR
R85	315-0222-00			2.2K OHM,0.25W,5%
R86	321-0313-00			17.8K OHM,0.125W,1%
R90	321-0296-00			11.8K OHM,0.125W,1%
R91	321-0342-00			35.7K OHM,0.125W,1%
R92	321-0239-00			3.01K OHM,0.125W,1%
R93	321-0259-00			4.87K OHM,0.125W,1%
R94	321-0259-00			4.87K OHM,0.125W,1%
R95	321-0289-00			10K OHM,0.125W,1%
R98	321-0355-00			48.7K OHM,0.125W,1%
R120	315-0472-00			4.7K OHM,0.25W,5%
R132	315-0391-00			390 OHM,0.25W,5%
R142	315-0472-00			4.7K OHM,0.25W,5%
R180	321-0318-00			20K OHM,0.125W,1%
R181	321-0347-00			40.2K OHM,0.125W,1%
R182	321-0318-00			20K OHM,0.125W,1%

[1]-02 only.

TC-1 (cont)

Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Description
RESISTORS (cont)				
R183	321-0289-00			10K OHM,0.125W,1%
R184	321-0347-00			40.2K OHM,0.125W,1%
R185	321-0376-00			80.6K OHM,0.125W,1%
R190	321-0225-00			2.15K OHM,0.125W,1%
R191	321-0252-00			4.12K OHM,0.125W,1%
R192	321-0309-00			16.2K OHM,0.125W,1%
R193	321-0251-00			4.02K OHM,0.125W,1%
R194	321-0280-00			8.06K OHM,0.125W,1%
R195	321-0222-00			2K OHM,0.125W,1%
R381	321-0254-00			4.32K OHM,0.125W,1%
R382	321-0292-00			10.7K OHM,0.125W,1%
R408	315-0472-00			4.7K OHM,0.25W,5%
R437	315-0150-00			15 OHM,0.25W,5%
R445	315-0475-00			4.7M OHM,0.25W,5%
R503	315-0301-00			300 OHM,0.25W,5%
R508	315-0472-00			4.7K OHM,0.25W,5%
R509	315-0472-00			4.7K OHM,0.25W,5%
R545	315-0273-00			27K OHM,0.25W,5%
R546	315-0472-00			4.7K OHM,0.25W,5%
R551	315-0472-00			4.7K OHM,0.25W,5%
INTEGRATED CIRCUITS				
U1	156-0174-00			DUAL 20MHZ J-K MASTER-SLAVE FLIP-FLOP, SN74111N
U7	156-0140-00			HEX. BUFFER/DRIVER,SN7417N
U20	156-0030-00			QUAD 2-INPUT POSITIVE NAND GATE,SN7400N
U27	156-0041-00			DUAL 15MHZ D-TYPE POS-EDGE-TRIG. FLIP-FLOP, SN7474N
U35	156-0150-00			QUAD 2-INPUT POSITIVE NAND BUFFER,SN7437N
U42	156-0032-00			SINGLE 10MHZ 1-&-3-BIT BINARY RIPPLE COUNTER, SN7493N
U50	156-0058-00			HEX. INVERTER,SN7404N
U65	156-0142-00			SINGLE 50MHZ DIVIDE-BY-2-&-8 RIPPLE COUNTER, SN74197N
U71	156-0042-00			DUAL 15MHZ J-K MASTER-SLAVE FLIP-FLOP, SN7476N
U80	156-0061-00			SINGLE BCD TO DECIMAL DECODER,SN7442N
U98	156-0067-00			OPERATIONAL AMPLIFIER,UA741C
U99	156-0067-00			OPERATIONAL AMPLIFIER,UA741C
U101	156-0035-00			SINGLE 8-INPUT POSITIVE NAND GATE,SN7430N
U107	156-0047-00			TRIPLE 3-INPUT POSITIVE NAND GATE,SN7410N
U113	156-0057-00			QUAD 2-INPUT POSITIVE NAND GATE,SN7401N
U126	156-0040-00			DUAL 2-BIT BISTABLE LATCH,SN7475N

TC-1 (cont)

Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Description
INTEGRATED CIRCUITS (cont)				
U159	156-0142-00			SINGLE 50MHZ DIVIDE-BY-2-&-8 RIPPLE COUNTER, SN74197N
U165	156-0142-00			SINGLE 50MHZ DIVIDE-BY-2-&-8 RIPPLE COUNTER, SN74197N
U171	156-0039-00			DUAL 15MHZ J-K MASTER-SLAVE FLIP-FLOP, SN7473N
U177	156-0143-00			SINGLE RETRIGGERABLE MONOSTABLE MULTI-VIBRATOR,SN74122N
U180	156-0112-00			QUAD 2-INPUT POSITIVE NAND GATE,SN7426N
U232	156-0144-00			TRIPLE 3-INPUT POSITIVE NAND GATE,SN7412N
U238	156-0150-00			QUAD 2-INPUT POSITIVE NAND BUFFER,SN7437N
U244	156-0039-00			DUAL 15MHZ J-K MASTER-SLAVE FLIP-FLOP, SN7473N
U253	156-0047-00			TRIPLE 3-INPUT POSITIVE NAND GATE,SN7410N
U259	156-0142-00			SINGLE 50MHZ DIVIDE-BY-2-&-8 RIPPLE COUNTER, SN74197N
U265	156-0043-00			QUAD 2-INPUT POSITIVE NOR GATE,SN7402N
U271	156-0129-00			QUAD 2-INPUT POSITIVE AND GATE,SN7408N
U277	156-0072-00			SINGLE MONOSTABLE MULTIVIBRATOR-ONE SHOT-, SN74121N
U281	156-0165-00			DUAL 4-INPUT POSITIVE NOR GATE,SN7425N
U289	156-0093-00			HEX. INVERTER,SN7416N
U296	156-0140-00			HEX. BUFFER/DRIVER,SN7417N
U305	156-0078-00			SINGLE 1-OUT-OF-16-LINE DECODER/DEMULTI-PLEXER,SN74154N
U316	156-0078-00			SINGLE 1-OUT-OF-16-LINE DECODER/DEMULTI-PLEXER,SN74154N
U326	156-0111-00			SINGLE BCD-TO-DECIMAL DECODER/DRIVER, SN74145N
U332	156-0043-00			QUAD 2-INPUT POSITIVE NOR GATE,SN7402N
U338	156-0057-00			QUAD 2-INPUT POSITIVE NAND GATE,SN7401N
U344	156-0143-00			SINGLE RETRIGGERABLE MONOSTABLE MULTI-VIBRATOR,SN74122N
U352	156-0034-00			DUAL 4-INPUT POSITIVE NAND GATE,SN7420N
U357	156-0035-00			SINGLE 8-INPUT POSITIVE NAND GATE,SN7430N
U363	156-0041-00			DUAL 15MHZ D-TYPE POS.-EDGE-TRIG. FLIP-FLOP, SN7474N
U371	156-0030-00			QUAD 2-INPUT POSITIVE NAND GATE,SN7400N
U377	156-0047-00			TRIPLE 3-INPUT POSITIVE NAND GATE,SN7410N
U390	156-0142-00			SINGLE 50MHZ DIVIDE-BY-2-&-8 RIPPLE COUNTER, SN74197N
U398	156-0142-00			SINGLE 50MHZ DIVIDE-BY-2-&-8 RIPPLE COUNTER, SN74197N
U450	156-0145-00			QUAD 2-INPUT POSITIVE NAND BUFFER,SN7438N
U457	156-0093-00			HEX. INVERTER,SN7416N

TC-1 (cont)

Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Description
INTEGRATED CIRCUITS (cont)				
U465	156-0296-00			MOS,READ ONLY MEMORY,24DIP
U479	156-0293-03			MOS,READ ONLY MEMORY,24DIP
U496	156-0299-00			16 BIT DATA SELECTOR,24DIP
U503	156-0058-00			HEX. INVERTER,SN7404N
U510	156-0041-00			DUAL 15MHZ D-TYPE POS.-EDGE-TRIG. FLIP-FLOP, SN7474N
U517	156-0035-00			SINGLE 8-INPUT POSITIVE NAND GATE,SN7430N
U524	156-0040-00			DUAL 2-BIT BISTABLE LATCH,SN7475N
U532	156-0040-00			DUAL 2-BIT BISTABLE LATCH,SN7475N
U538	156-0030-00			QUAD 2-INPUT POSITIVE NAND GATE,SN7400N
U557	307-0387-00			8.2K OHM,13 RESISTOR NETWORK,FILM
CRYSTAL				
Y153	158-0072-00			4.9152MHZ

A2 ASSEMBLY TC-2

Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Description
ASSEMBLIES				
A2	670-1729-02	B010100	B029999	CIRCUIT CARD ASSEMBLY, TC-2
A2	670-1729-04	B030000		CIRCUIT CARD ASSEMBLY, TC-2
	670-3084-00	XB030000		CIRCUIT BOARD ASSEMBLY, Z CONTROL
CAPACITORS				
C60	285-0596-00			0.01UF,PTM,100V,1%
C61	285-0596-00			0.01UF,PTM,100V,1%
C62	281-0525-00			470PF,CER,500V,20%
C63	290-0512-00			22UF,ELECT.,15V,20%
C70	285-0596-00			0.01UF,PTM,100V,1%
C71	285-0596-00			0.01UF,PTM,100V,1%
C72	281-0525-00			470PF,CER,500V,20%
C77	290-0512-00			22UF,ELECT.,15V,20%
C81	290-0523-00			2.2UF,ELECT.,20V,20%
C82	283-0068-00			0.01UF,CER,500V,+100-0%
C86	281-0658-00			6.2PF,CER,500V,±0.25PF
C88	283-0203-00			0.47UF,CER,50V,20%
C94	283-0068-00			0.01UF,CER,500V,+100-0%
C96	283-0068-00			0.01UF,CER,500V,+100-0%
C97	283-0068-00			0.01UF,CER,500V,+100-0%
C98	283-0068-00			0.01UF,Cer,500V,+100-0%
DIODES,SILICON				
CR5	152-0141-02			1N4152
CR6	152-0141-02			1N4152
CR7	152-0141-02			1N4152
CR8	152-0141-02			1N4152
CR9	152-0141-02			1N4152

TC-2 (cont)

Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Description
DIODES,SILICON (cont)				
CR15	152-0141-02			1N4152
CR16	152-0141-02			1N4152
CR17	152-0141-02			1N4152
CR18	152-0141-02			1N4152
CR19	152-0141-02			1N4152
CR35	152-0141-02			1N4152
CR36	152-0141-02			1N4152
CR37	152-0141-02			1N4152
CR38	152-0141-02			1N4152
CR39	152-0141-02			1N4152
CR45	152-0141-02			1N4152
CR46	152-0141-02			1N4152
CR47	152-0141-02			1N4152
CR48	152-0141-02			1N4152
CR49	152-0141-02			1N4152
CR90	152-0141-02			1N4152
TRANSISTORS				
Q1	151-0302-00			SILICON,NPN,2N2222A
Q41	151-0302-00			SILICON,NPN,2N2222A
Q43[1]	151-1042-00			SILICON,JFET,N CHANNEL,2N5245 (MATCHED PAIR)
Q45	151-0188-00			SILICON,PNP,2N3906
Q47[1]	151-1042-00			SILICON,JFET,N CHANNEL,2N5245 (MATCHED PAIR)
RESISTORS				
R3	315-0473-00			47K OHM,0.25W,5%
R4	321-0272-00			6.65K OHM,0.125W,1%
R5	323-0510-00			2M OHM,0.50W,1%
R6	322-0693-00			1.036M OHM,0.25W,1%
R7	322-0694-00			517.1K OHM,0.25W,1%
R8	322-0695-00			258.2K OHM,0.25W,1%
R9	322-0696-00			128.93K OHM,0.25W,1%
R15	322-0697-02			64.374K OHM,0.25W,1%
R16	308-0697-00			32.14K OHM,0.125W,WW,0.1%
R17	308-0698-00			16.046K OHM,0.125W,WW,0.1%
R18	308-0699-00			8.115K OHM,0.125W,WW,0.1%
R19	308-0658-00			4K OHM,0.125W,WW,0.01%
R21	315-0472-00			4.7K OHM,0.25W,5%
R23	321-0221-00			1.96K OHM,0.125W,1%
R25	315-0222-00			2.2K OHM,0.25W,5%
R26	315-0101-00			100 OHM,0.25W,5%
R28	321-0210-00			1.5K OHM,0.125W,1%
R33	315-0473-00			47K OHM,0.25W,5%

[1]Matched pair.

TC-2 (cont)

Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Description
RESISTORS (cont)				
R34	321-0261-00			5.11K OHM,0.125W,1%
R35	323-0510-00			2M OHM,0.50W,1%
R36	322-0693-00			1.036M OHM,0.25W,1%
R37	322-0694-00			517.1K OHM,0.25W,1%
R38	322-0695-00			258.2K OHM,0.25W,1%
R39	322-0696-00			128.93K OHM,0.25W,1%
R45	322-0697-02			64.374K OHM,0.25W,5%
R46	308-0697-00			32.14K OHM,0.125W,WW,0.1%
R47	308-0698-00			16.046K OHM,0.125W,WW,0.1%
R48	308-0699-00			8.115K OHM,0.125W,WW,0.1%
R49	308-0658-00			4K OHM,0.125W,WW,0.01%
R51	315-0472-00			4.7K OHM,0.25W,5%
R53	321-0315-00			18.7K OHM,0.125W,1%
R54	321-0289-00			10K OHM,0.125W,1%
R56	315-0473-00			47K OHM,0.25W,5%
R58	315-0472-00			4.7K OHM,0.25W,5%
R60	321-0365-00			61.9K OHM,0.125W,1%
R61	321-0365-00			61.9K OHM,0.125W,1%
R62	321-0403-00			154K OHM,0.125W,1%
R65	315-0472-00			4.7K OHM,0.25W,5%
R67	315-0473-00			47K OHM,0.25W,5%
R70	321-0365-00			61.9K OHM,0.125W,1%
R71	321-0365-00			61.9K OHM,0.125W,1%
R72	321-0403-00			154K OHM,0.125W,1%
R75	321-0315-00			18.7K OHM,0.125W,1%
R76	321-0289-00			10K OHM,0.125W,1%
R78	315-0473-00			47K OHM,0.25W,5%
R80	315-0472-00			4.7K OHM,0.25W,5%
R85	311-1134-00			50K OHM,VAR
R86	315-0102-00			1K OHM,0.25W,5%
R90	315-0472-00			4.7K OHM,0.25W,5%
R91	315-0472-00			4.7K OHM,0.25W,5%
R92	315-0472-00			4.7K OHM,0.25W,5%
R93	315-0472-00			4.7K OHM,0.25W,5%
R96	315-0102-00			1K OHM,0.25W,5%
R98	315-0472-00			4.7K OHM,0.25W,5%
INTEGRATED CIRCUITS				
U1	156-0145-00			QUAD 2-INPUT POSITIVE NAND BUFFER, SN7438N
U3	156-0072-00			SINGLE MONOSTABLE MULTIVIBRATOR-ONE-SHOT-,SN74121N
U5	156-0072-00			SINGLE MONOSTABLE MULTIVIBRATOR-ONE-SHOT-,SN74121N

TC-2 (cont)

Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Description
INTEGRATED CIRCUITS (cont)				
U7	156-0075-00			SINGLE 8-BIT DATA SELECTOR/MULTI-PLEXER,SN74151N
U9	156-0075-00			SINGLE 8-BIT DATA SELECTOR/MULTI-PLEXER,SN74151N
U10	156-0075-00			SINGLE 8-BIT DATA SELECTOR/MULTI-PLEXER,SN74151N
U11	156-0075-00			SINGLE 8-BIT DATA SELECTOR/MULTI-PLEXER,SN74151N
U12	156-0075-00			SINGLE 8-BIT DATA SELECTOR/MULTI-PLEXER,SN74151N
U13	156-0058-00			HEX. INVERTER,SN7404N
U15	156-0106-00			MONOLITHIC 6-DIODE ARRAY,RCA3039
U17	156-0106-00			MONOLITHIC 6-DIODE ARRAY,RCA3039
U19	156-0067-00			OPERATIONAL AMPLIFIER,UA741C
U21	156-0072-00			SINGLE MONOSTABLE MULTIVIBRATOR-ONE-SHOT-,SN74121N
U23	156-0039-00			DUAL 15MHZ J-K MASTER-SLAVE FLIP-FLOP, SN7473N
U25	156-0047-00			TRIPLE 3-INPUT POSITIVE NAND GATE, SN7410N
U27	156-0042-00			DUAL 15MHZ J-K MASTER-SLAVE FLIP-FLOP, SN7476N
U29	156-0039-00			DUAL 15MHZ J-K MASTER-SLAVE FLIP-FLOP, SN7473N
U31	156-0061-00			SINGLE BCD TO DECIMAL DECODER,SN7442N
U33	156-0145-00			QUAD 2-INPUT POSITIVE NAND BUFFER, SN7438N
U34	156-0032-00			SINGLE 10MHZ 1-&-3-BIT BINARY RIPPLE COUNTER,SN7493N
U35	156-0089-00			SINGLE 25MHZ SYNC. 4-BIT UP/DOWN COUNTER, SN74193N
U36	156-0089-00			SINGLE 25MHZ SYNC. 4-BIT UP/DOWN COUNTER, SN74193N
U37	156-0058-00			HEX. INVERTER,SN7404N
U38	156-0067-00			OPERATIONAL AMPLIFIER,UA741C
U39	156-0067-00			OPERATIONAL AMPLIFIER,UA741C
U41	156-0039-00			DUAL 15MHZ J-K MASTER-SLAVE FLIP-FLOP, SN7473N
U42	156-0041-00			DUAL 15MHZ D-TYPE POS.-EDGE-TRIG. FLIP-FLOP,SN7474N
U43	156-0030-00			QUAD 2-INPUT POSITIVE NAND GATE,SN7400N
U44	156-0145-00			QUAD 2-INPUT POSITIVE NAND BUFFER,SN7438N
U45	156-0057-00			QUAD 2-INPUT POSITIVE NAND GATE,SN7401N
U47	156-0043-00			QUAD 2-INPUT POSITIVE NOR GATE,SN7402N

TC-2 (cont)

Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Description
INTEGRATED CIRCUITS (cont)				
U48	156-0041-00			DUAL 15MHZ D-TYPE POS.-EDGE-TRIG. FLIP-FLOP,SN7474N
U49	156-0040-00			DUAL 2-BIT BISTABLE LATCH,SN7475N
U51	156-0089-00			SINGLE 25MHZ SYNC. 4-BIT UP/DOWN COUNTER, SN74193N
U53	156-0089-00			SINGLE 25MHZ SYNC. 4-BIT UP/DOWN COUNTER, SN74193N
U55	156-0089-00			SINGLE 25MHZ SYNC. 4-BIT UP/DOWN COUNTER, SN74193N
U57	156-0106-00			MONOLITHIC, 6-DIODE ARRAY,RCA3039
U59	156-0106-00			MONOLITHIC, 6-DIODE ARRAY,RCA3039
U61	156-0034-00			DUAL 4-INPUT POSITIVE NAND GATE,SN7420N
U62	156-0039-00			DUAL 15MHZ J-K MASTER-SLAVE FLIP-FLOP, SN7473N
U63	156-0030-00			QUAD 2-INPUT POSITIVE NAND GATE,SN7400N
U64	156-0030-00			QUAD 2-INPUT POSITIVE NAND GATE,SN7400N
U65	156-0145-00			QUAD 2-INPUT POSITIVE NAND BUFFER,SN7438N
U66	156-0144-00			TRIPLE 3-INPUT POSITIVE NAND GATE,SN7412N
U67	156-0129-00			QUAD 2-INPUT POSITIVE AND GATE,SN7408N
U68	156-0030-00			Quad 2-INPUT POSITIVE NAND GATE,SN7400N
U69	156-0047-00			TRIPLE 3-INPUT POSITIVE NAND GATE,SN7410N
U70	156-0058-00			HEX. INVERTER,SN7404N
U71	156-0089-00			SINGLE 25MHZ SYNC. 4-BIT UP/DOWN COUNTER, SN74193N
U73	156-0152-00			DUAL 5-BIT BUFFER REGISTER,N8201N
U75	156-0105-00			OPERATIONAL AMPLIFIER,LM301AN
U77	156-0067-00			OPERATIONAL AMPLIFIER,UA741C
U79	156-0067-00			OPERATIONAL AMPLIFIER,UA741C
	670-3084-00	XB030000		CIRCUIT BOARD ASSEMBLY, Z CONTROL
CAPACITORS				
C1	283-0000-00			0.001UF,CER,500V,+100-0%
C17	283-0000-00			0.001UF,CER,500V,+100-0%
C44	283-0000-00			0.001UF,CER,500V,+100-0%
TRANSISTORS				
Q6	151-0126-00			SILICON,NPN,SELECTED FROM 2N2484
Q8	151-0410-00			SILICON,PNP,2N5087
Q11	151-1025-00			SILICON,JFET,N CHANNEL,2N5245
Q12	151-0126-00			SILICON,NPN,SELECTED FROM 2N2484
Q15	151-0410-00			SILICON,PNP,2N5087
RESISTORS				
R2	315-0681-00			680 OHM,0.25W,5%
R3	315-0303-00			30K OHM,0.25W,5%
R7	315-0473-00			47K OHM,0.25W,5%
R8	315-0681-00			680 OHM,0.25W,5%

Z CONTROL (cont)

Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Description
RESISTORS (cont)				
R14	315-0203-00			20K OHM,0.25W,5%
R16	315-0303-00			30K OHM,0.25W,5%
R38	315-0472-00			47K OHM,0.25W,5%
R39	315-0472-00			47K OHM,0.25W,5%
R45	315-0153-00			15K OHM,0.25W,5%
INTEGRATED CIRCUITS				
U21	156-0047-00			TRIPLE 3-INPUT POSITIVE NAND GATE, SN7410N
U31	156-0145-00			QUAD 2-INPUT POSITIVE NAND BUFFER, SN7438N
U41	156-0072-00			SINGLE MONOSTABLE MULTIVIBRATOR-ONE SHOT-,SN74121N

A2 ASSEMBLY TC-2

Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Description
ASSEMBLIES				
A2	670-1729-05			CIRCUIT CARD ASSEMBLY, TC-2
A2	670-1729-06			CIRCUIT CARD ASSEMBLY, TC-2
CAPACITORS				
C9	283-0068-00			0.01UF,CER,500V,+100-0%
C26[1]	281-0543-00			270PF,CER,500V,10%
C31[1]	281-0504-00			10PF,CER,500V,±1%
C38	281-0546-00			330PF,CER,500V,10%
C84	290-0512-00			22UF,ELECT.,15V,20%
C88	285-0596-00			0.01UF,PTM,100V,1%
C89	285-0596-00			0.01UF,PTM,100V,1%
C90	281-0525-00			470PF,CER,500V,20%
C149	283-0068-00			0.01UF,CER,500V,+100-0%
C171	283-0068-00			0.01UF,CER,500V,+100-0%
C174	285-0596-00			0.01UF,PTM,100V,1%
C175	285-0596-00			0.01UF,PTM,100V,1%
C176	281-0525-00			470PF,CER,500V,20%
C201	283-0068-00			0.01UF,CER,500V,+100-0%
C202	290-0523-00			2.2UF,ELECT.,20V,20%
C209	283-0068-00			0.01UF,CER,500V,+100-0%
C241	283-0000-00			0.001UF,CER,500V,+100-0%
C276	290-0512-00			22UF,ELECT.,15V,20%
C280	290-0512-00			22UF,ELECT.,15V,20%
C282	283-0000-00			0.001UF,CER,500V,+100-0%
C286	283-0000-00			0.001UF,CER,500V,+100-0%
C301	283-0203-00			0.47UF,CER,50V,20%
C329	283-0068-00			0.01UF,CER,500V,+100-0%
C359	283-0068-00			0.01UF,CER,500V,+100-0%

[1]-06 only.

TC 2 (cont).

Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Description
DIODES				
CR28[1]	152-0075-00			GERMANIUM,GD238 OR ED48
CR180	152-0141-02			SILICON,1N4152
CR181	152-0141-02			SILICON,1N4152
CR182	152-0141-02			SILICON,1N4152
CR183	152-0141-02			SILICON,1N4152
CR185	152-0141-02			SILICON,1N4152
CR186	152-0141-02			SILICON,1N4152
CR187	152-0141-02			SILICON,1N4152
CR188	152-0141-02			SILICON,1N4152
CR189	152-0141-02			SILICON,1N4152
CR190	152-0141-02			SILICON,1N4152
CR283	152-0141-02			SILICON,1N4152
CR285	152-0141-02			SILICON,1N4152
CR381	152-0141-02			SILICON,1N4152
CR382	152-0141-02			SILICON,1N4152
CR383	152-0141-02			SILICON,1N4152
CR384	152-0141-02			SILICON,1N4152
CR385	152-0141-02			SILICON,1N4152
CR386	152-0141-02			SILICON,1N4152
CR387	152-0141-02			SILICON,1N4152
CR388	152-0141-02			SILICON,1N4152
CR389	152-0141-02			SILICON,1N4152
TRANSISTORS				
Q77	151-0302-00			SILICON,NPN,2N2222A
Q78	151-0302-00			SILICON,NPN,2N2222A
Q79	151-0188-00			SILICON,PNP,2N3906
Q80	151-1078-00			SILICON,JFET,N-CHANNEL
Q85	151-1078-00			SILICON,JFET,N-CHANNEL
Q273	151-1025-00			SILICON,JFET,N-CHANNEL
Q274	151-0410-00			SILICON,PNP,SELECTED FROM 2N5087
Q275	151-0126-00			SILICON,NPN,SELECTED FROM 2N2484
Q277	151-0410-00			SILICON,PNP,SELECTED FROM 2N5087
Q278	151-0126-00			SILICON,NPN,SELECTED FROM 2N2484
RESISTORS				
R27[1]	315-0152-00			1.5K OHM,0.25W,5%
R29	311-1134-00			5K OHM,VAR
R30[1]	315-0244-00			240K OHM,0.25W,5%
R31[2]	315-0102-00			1K OHM,0.25W,5%
R31[1]	315-0302-00			3K OHM,0.25W,5%
R39	315-0332-00			3.3K OHM,0.25W,5%
R72	315-0472-00			4.7K OHM,0.25W,5%
R73	321-0315-00			18.7K OHM,0.125W,1%
R74	321-0289-00			10K OHM,0.125W,1%
R75	315-0472-00			4.7K OHM,0.25W,5%

[1]-06 only.
[2]-05 only.

TC-2 (cont)

Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Description
RESISTORS (Cont)				
R76	315-0473-00			47K OHM,0.25W,5%
R77	315-0472-00			4.7K OHM,0.25W,5%
R83	315-0473-00			47K OHM,0.25W,5%
R86	308-0697-00			32.14K OHM,0.125W,WW,0.1%
R87	321-0365-00			61.9K OHM,0.125W,1%
R88	321-0403-00			154K OHM,0.125W,1%
R89	321-0365-00			61.9K OHM,0.125W,1%
R90	315-0106-00			10M OHM,0.25W,5%
R175	315-0106-00			10M OHM,0.25W,5%
R176	321-0365-00			61.9K OHM,0.125W,1%
R177	321-0403-00			154K OHM,0.125W,1%
R178	321-0365-00			61.9K OHM,0.125W,1%
R182	308-0698-00			16.046K OHM,0.125W,WW,0.1%
R183	308-0658-00			4K OHM,0.125W,WW,0.01%
R186	308-0699-00			8.115K OHM,0.125W,WW,0.1%
R187	315-0303-00			30K OHM,0.25W,5%
R191	322-0696-00			128.93K OHM,0.25W,1%
R192	323-0510-00			2M OHM,0.50W,1%
R193	322-0693-00			1.036M OHM,0.25W,1%
R194	322-0694-00			517.1K OHM,0.25W,1%
R195	322-0697-02			64.374K OHM,0.25W,0.5%
R196	322-0695-00			258.2K OHM,0.25W,1%
R201	315-0102-00			1K OHM,0.25W,5%
R241	315-0153-00			15K OHM,0.25W,5%
R261	315-0472-00			4.7K OHM,0.25W,5%
R264	315-0472-00			4.7K OHM,0.25W,5%
R265	315-0472-00			4.7K OHM,0.25W,5%
R273	315-0473-00			47K OHM,0.25W,5%
R274	321-0315-00			18.7K OHM,0.125W,1%
R275	321-0289-00			10K OHM,0.125W,1%
R276	321-0318-00			20K OHM,0.125W,1%
R277	315-0473-00			47K OHM,0.25W,5%
R278	315-0303-00			30K OHM,0.25W,5%
R280	315-0681-00			680 OHM,0.25W,5%
R281	315-0681-00			680 OHM,0.25W,5%
R283	321-0261-00			5.11K OHM,0.125W,1%
R284	315-0473-00			47K OHM,0.25W,5%
R285	321-0210-00			1.5K OHM,0.125W,1%
R286	315-0101-00			100 OHM,0.25W,5%
R287	315-0222-00			2.2K OHM,0.25W,5%
R288	315-0473-00			47K OHM,0.25W,5%
R289	321-0272-00			6.65K OHM,0.125W,1%
R290	321-0221-00			1.96K OHM,0.125W,1%
R303	315-0472-00			4.7K OHM,0.25W,5%
R309	315-0472-00			4.7K OHM,0.25W,5%

TC-2 (cont)

Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Description
RESISTORS (cont)				
R331	315-0472-00			4.7K OHM,0.25W,5%
R345	315-0472-00			4.7K OHM,0.25W,5%
R349	315-0472-00			4.7K OHM,0.25W,5%
R380	308-0697-00			32.14K OHM,0.125W,WW,0.1%
R381	308-0698-00			16.046K OHM,0.125W,WW,0.1%
R382	308-0699-00			8.115K OHM,0.125W,WW,0.1%
R387	308-0658-00			4K OHM,0.125W,WW,0.01%
R391	322-0697-02			64.374K OHM,0.25W,0.5%
R392	322-0696-00			128.93K OHM,0.25W,1%
R393	323-0510-00			2M OHM,0.50W,1%
R394	322-0693-00			1.036M OHM,0.25W,1%
R395	322-0694-00			517.1K OHM,0.25W,1%
R396	322-0695-00			258.2K OHM,0.25W,1%
INTEGRATED CIRCUITS				
U9	156-0041-00			DUAL 15MHZ D-TYPE POS.-EDGE-TRIG. FILP-FLOP,SN7474N
U31	156-0172-00			DUAL RETRIGGERABLE MONOSTABLE MULTIVIBRATOR,SN74123N
U39	156-0039-00			DUAL 15MHZ J-K MASTER-SLAVE FLIP-FLOP, SN7473N
U41	156-0032-00			SINGLE 10MHZ 1-&-3-BIT BINARY RIPPLE COUNTER,SN7493N
U49	156-0061-00			SINGLE BCD TO DECIMAL DECODER,SN7442N
U51	156-0075-00			SINGLE 8-BIT DATA SELECTOR/MULIPLEXER, SN74151N
U59	156-0075-00			SINGLE 8-BIT DATA SELECTOR/MULTIPLEXER, SN74151N
U61	156-0089-00			SINGLE 25MHZ SYNC. 4-BIT UP/DOWN COUNTER, SN74193N
U69	156-0089-00			SINGLE 25MHZ SYNC. 4-BIT UP/DOWN COUNTER, SN74193N
U71	156-0089-00			SINGLE 25MHZ SYNC. 4-BIT UP/DOWN COUNTER, SN74193N
U91	156-0105-00			OPERATIONAL AMPLIFIER,LM301AN
U92	156-0067-07			OPERATIONAL AMPLIFIER,UA741C
U109	156-0030-00			QUAD 2-INPUT POSITIVE NAND GATE,SN7400N
U129	156-0039-00			DUAL 15MHZ J-K MASTER-SLAVE FLIP-FLOP, SN7473N
U131	156-0039-00			DUAL 15MHZ J-K MASTER-SLAVE FLIP-FLOP, SN7473N
U139	156-0030-00			QUAD 2-INPUT POSITIVE AND GATE,SN7400N
U141	156-0047-00			TRIPLE 3-INPUT POSITIVE NAND GATE,SN7410N
U149	156-0047-00			TRIPLE 3-INPUT POSITIVE NAND GATE,SN7410N
U151	156-0075-00			SINGLE 8-BIT DATA SELECTOR/MULTIPLEXER, SN74151N

TC-2 (cont)

Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Description
INTEGRATED CIRCUITS (cont)				
U159	156-0075-00			SINGLE 8-BIT DATA SELECTOR/MULTIPLEXER, SN74151N
U161	156-0075-00			SINGLE 8-BIT DATA SELECTOR/MULTIPLEXER, SN74151N
U169	156-0040-00			DUAL 4-BIT BISTABLE LATCH,SN7475N
U171	156-0041-00			DUAL 15MHZ D-TYPE POS.-EDGE-TRIG. FLIP-FLOP,SN7474N
U179	156-0067-07			OPERATIONAL AMPLIFIER,UA741C
U181	156-0067-07			OPERATIONAL AMPLIFIER,UA741C
U189	156-0106-00			MONOLITHIC,6 DIODE ARRAY,RCA3019
U191	156-0106-00			MONOLITHIC,6 DIODE ARRAY,RCA3019
U201	156-0072-00			SINGLE MONOSTABLE MULTIVIBRATOR,ONE SHOT, SN74121N
U209	156-0030-00			QUAD 2-INPUT POSITIVE NAND GATE,SN7400N
U229	156-0039-00			DUAL 15MHZ J-K MASTER-SLAVE FLIP-FLOP, SN7473N
U231	156-0034-00			DUAL 4-INPUT POSITIVE NAND GATE,SN7420N
U239	156-0043-00			QUAD 2-INPUT POSITIVE NOR GATE,SN7402N
U241	156-0072-00			SINGLE MONOSTABLE MULTIVIBRATOR,ONE SHOT, SN74121N
U249	156-0030-00			QUAD 2-INPUT POSITIVE NAND GATE,SN7400N
U251	156-0058-00			HEX. INVERTER,SN7404N
U259	156-0030-00			QUAD 2-INPUT POSITIVE NAND GATE,SN7400N
U261	156-0144-00			TRIPLE 3-INPUT POSITIVE NAND GATE,SN7412N
U271	156-0152-00			DUAL 5-BIT BUFFER REGISTER,SN8201N
U291	156-0067-07			OPERATIONAL AMPLIFIER,UA741C
U292	156-0067-07			OPERATIONAL AMPLIFIER,UA741C
U301	156-0072-00			SINGLE MONOSTABLE MULTIVIBRATOR,ONE SHOT, SN74121N
U309	156-0145-00			QUAD 2-INPUT POSITIVE NAND BUFFER,SN7438N
U329	156-0030-00			QUAD 2-INPUT POSITIVE NAND GATE,SN7400N
U331	156-0042-00			DUAL 15MHZ J-K MASTER-SLAVE FLIP-FLOP, SN7476N
U339	156-0145-00			QUAD 2-INPUT POSITIVE NAND BUFFER,SN7438N
U341	156-0057-00			QUAD 2-INPUT POSITIVE NAND GATE,SN7401N
U349	156-0129-00			QUAD 2-INPUT POSITIVE NAND GATE,SN7408N
U351	156-0145-00			QUAD 2-INPUT POSITIVE NAND BUFFER,SN7438N
U359	156-0145-00			QUAD 2-INPUT POSITIVE NAND BUFFER,SN7438N
U361	156-0089-00			SINGLE 25MHZ 4-BIT UP/DOWN COUNTER,SN74193N
U369	156-0089-00			SINGLE 25MHZ 4-BIT UP/DOWN COUNTER,SN74193N
U371	156-0089-00			SINGLE 25MHZ 4-BIT UP/DOWN COUNTER,SN74193N
U378	156-0058-00			HEX. INVERTER,SN7404N
U379	156-0058-00			HEX. INVERTER,SN7404N
U389	156-0106-00			MONOLITHIC,6 DIODE ARRAY,RCA3039
U391	156-0106-00			MONOLITHIC,6 DIODE ARRAY,RCA3039

Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Description
				A3 ASSEMBLY MOTHER
ASSEMBLY				
A3	670-2360-01			CIRCUIT BOARD ASSEMBLY, MOTHER
CAPACITOR				
C79	283-0068-00			0.01UF,CER,500V,+100-0%
DIODES,SILICON				
CR39	152-0066-00			DIFFUSED,SELECTED FROM 1N3194
CR75	152-0141-02			1N4152
CONNECTORS				
J30	131-0589-00			TERMINAL,PIN
J31	131-0589-00			TERMINAL,PIN
J32	131-0589-00			TERMINAL,PIN
J33	131-0589-00			TERMINAL,PIN
J34	131-0589-00			TERMINAL,PIN
RESISTORS				
R5	315-0182-00			1.8K OHM,0.25W,5%
R7	315-0681-00			680 OHM,0.25W,5%
R9	315-0182-00			1.8K OHM,0.25W,5%
R11	315-0182-00			1.8K OHM,0.25W,5%
R13	315-0681-00			680 OHM,0.25W,5%
R15	315-0182-00			1.8K OHM,0.25W,5%
R16	315-0182-00			1.8K OHM,0.25W,5%
R17	315-0182-00			1.8K OHM,0.25W,5%
R18	315-0182-00			1.8K OHM,0.25W,5%
R19	315-0471-00			470 OHM,0.25W,5%
R21	315-0182-00			1.8K OHM,0.25W,5%
R23	315-0471-00			470 OHM,0.25W,5%
R24	315-0182-00			1.8K OHM,0.25W,5%
R25	315-0182-00			1.8K OHM,0.25W,5%

MOTHER BOARD (cont)

Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Description
RESISTORS (cont)				
R27	315-0182-00			1.8K OHM,0.25W,5%
R28	315-0182-00			1.8K OHM,0.25W,5%
R29	315-0182-00			1.8K OHM,0.25W,5%
R31	315-0681-00			680 OHM,0.25W,5%
R33	315-0471-00			470 OHM,0.25W,5%
R35	315-0182-00			1.8K OHM,0.25W,5%
R37	315-0182-00			1.8K OHM,0.25W,5%
R41	315-0182-00			1.8K OHM,0.25W,5%
R43	315-0182-00			1.8K OHM,0.25W,5%
R45	315-0182-00			1.8K OHM,0.25W,5%
R46	315-0182-00			1.8K OHM,0.25W,5%
R47	315-0182-00			1.8K OHM,0.25W,5%
R48	315-0182-00			1.8K OHM,0.25W,5%
R49	315-0681-00			680 OHM,0.25W,5%
R51	315-0182-00			1.8K OHM,0.25W,5%
R53	315-0182-00			1.8K OHM,0.25W,5%
R54	315-0681-00			680 OHM,0.25W,5%
R55	315-0471-00			470 OHM,0.25W,5%
R57	315-0182-00			1.8K OHM,0.25W,5%
R61	315-0182-00			1.8K OHM,0.25W,5%
R62	315-0182-00			1.8K OHM,0.25W,5%
R63	315-0182-00			1.8K OHM,0.25W,5%
R65	315-0681-00			680 OHM,0.25W,5%
R67	315-0182-00			1.8K OHM,0.25W,5%
R69	315-0182-00			1.8K OHM,0.25W,5%
R71	315-0182-00			1.8K OHM,0.25W,5%
R73	315-0182-00			1.8K OHM,0.25W,5%
R75	315-0182-00			1.8K OHM,0.25W,5%
R77	315-0182-00			1.8K OHM,0.25W,5%

A4 ASSEMBLY DEFLECTION AMP & STORAGE

Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Description
ASSEMBLIES				
A4	670-2571-00	B010100	B010104	CIRCUIT BOARD ASSEMBLY, DEFLECTION AMPL & STORAGE
A4	670-2571-01	B010105	B010124	CIRCUIT BOARD ASSEMBLY, DEFLECTION AMPL & STORAGE
A4	670-2571-02	B010125	B029999	CIRCUIT BOARD ASSEMBLY, DEFLECTION AMPL & STORAGE
A4	670-2571-03	B030000		CIRCUIT BOARD ASSEMBLY, DEFLECTION AMPL & STORAGE
A4	670-2571-04			CIRCUIT BOARD ASSEMBLY, DEFLECTION AMPL & STORAGE
CAPACITORS				
C106	283-0220-00	XB010125		0.01UF,CER,50V,20%
C108	283-0239-00			0.022UF,CER,50V,10%

DEFLECTION AMPL & STORAGE (cont)

Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Description
CAPACITORS (cont)				
C114	281-0510-00	XB030000		22PF,CER,500V,20%
C134	283-0023-00			0.1UF,CER,10V,+80-20%
C139	290-0536-00			10UF,ELECT.,25V,20%
C169[1]	283-0000-00			0.001UF,CER,500V,+80-20%
C192	290-0536-00			10UF,ELECT.,25V,20%
C237	283-0239-00			0.022UF,CER,50V,10%
C238	283-0220-00	XB010125		0.01UF,CER,50V,20%
C239	290-0536-00			10UF,ELECT.,25V,20%
C240	283-0220-00	XB010125		0.01UF,CER,50V,20%
C242	283-0220-00			0.01UF,CER,50V,20%
C243	283-0220-00			0.01UF,CER,50V,20%
C270[1]	283-0110-00			0.005UF,CER,150V
C271	283-0068-00			0.01UF,CER,500V,+100-0%
C279	290-0536-00			10UF,ELECT.,25V,20%
C289	290-0536-00			10UF,ELECT.,25V,20%
C317	281-0550-00			120PF,CER,500V,10%
C331	281-0550-00			120PF,CER,500V,10%
C419	281-0622-00			47PF,CER,500V,1%
C462	290-0267-00			1UF,ELECT.,35V
C470	283-0000-00			0.001UF,CER,500V,+80-20%
C472[1]	290-0536-00			10UF,ELECT.,25V,20%
C476	283-0068-00			0.01UF,CER,500V,+100-0%
C486	281-0550-00			120PF,CER,500V,10%
C524	281-0622-00			47PF,CER,500V,1%
C543	290-0536-00	B010100	B010124	10UF,ELECT.,25V,20%
C543	290-0517-00	B010125		6.8UF,ELECT.,35V,20%
C549[1]	283-0010-00			0.05UF,CER,50V
C557	281-0550-00			120PF,CER,500V,10%
C576	281-0550-00			120PF,CER,500V,10%
C585	283-0068-00			0.01UF,CER,500V,+100-0%
C595	283-0068-00			0.01UF,CER,500V,+100-0%
C598	290-0260-00			50UF,ELECT.,200V
C618	281-0622-00			47PF,CER,500V,1%
C643	290-0536-00	B010100	B010124	10UF,ELECT.,25V,20%
C643	290-0517-00	B010125		6.8UF,ELECT.,35V,20%
C654[1]	283-0000-00			0.001UF,CER,500V,+100-0%
C665	290-0536-00			10UF,ELECT.,25V,20%
C667	290-0536-00			10UF,ELECT.,25V,20%
C670	290-0536-00			10UF,ELECT.,25V,20%
C674	283-0068-00			0.01UF,CER,500V,+100-0%
C675	283-0068-00			0.01UF,CER,500V,+100-0%
C680	283-0068-00			0.01UF,CER,500V,+100-0%

[1]-00,-01,-02,-03 only.

DEFLECTION AMPL & STORAGE (cont)

Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Description
CAPACITORS (cont)				
C688	283-0128-00			100PF,CER,500V,5%
C690	283-0128-00			100PF,CER,500V,5%
DIODES,SILICON				
CR116	152-0141-02			1N4152
CR117	152-0141-02			1N4152
CR128	152-0141-02			1N4152
CR129	152-0141-02			1N4152
CR146	152-0141-02			1N4152
CR186	152-0141-02			1N4152
CR247	152-0141-02			1N4152
CR257	152-0141-02			1N4152
CR258	152-0141-02			1N4152
CR273	152-0141-02			1N4152
CR347	152-0141-02			1N4152
CR431	152-0141-02			1N4152
CR432	152-0141-02			1N4152
CR434	152-0141-02			1N4152
CR435	152-0141-02			1N4152
CR436	152-0141-02			1N4152
CR437	152-0141-02			1N4152
CR438	152-0141-02			1N4152
CR439	152-0141-02			1N4152
CR447	152-0141-02			1N4152
CR456	152-0141-02			1N4152
CR457	152-0141-02			1N4152
CR547	152-0141-02			1N4152
CR548	152-0141-02			1N4152
CR592	152-0107-00			TI60 or 1N647
CR680	152-0141-02			1N4152
CR687	152-0141-02			1N4152
CR690	152-0107-00			TI60 or 1N647
CR695	152-0141-02			1N4152
TRANSISTORS				
Q97	151-0149-00			SILICON,NPN,TEK SPEC
Q114	151-0136-00			SILICON,NPN,2N3053
Q132	151-0136-00			SILICON,NPN,2N3053
Q182	151-0219-00			SILICON,PNP,2N4250
Q183	151-0341-00			SILICON,NPN,2N3565
Q215	151-0134-00			SILICON,PNP,2N2905A
Q233	151-0134-00			SILICON,PNP,2N2905A
Q279	151-0341-00			SILICON,NPN,2N3565
Q288	151-0219-00			SILICON,PNP,2N4250

DEFLECTION AMPL & STORAGE (cont)

Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Description
TRANSISTORS (cont)				
Q291	151-0341-00			SILICON,NPN,2N3565
Q385	151-0219-00			SILICON,PNP,2N4250
Q386	151-0219-00			SILICON,PNP,2N4250
Q445	151-0188-00			SILICON,PNP,2N3906
Q448	151-0188-00			SILICON,PNP,2N3906
Q473	151-0219-00			SILICON,PNP,2N4250
Q474	151-0169-00			SILICON,NPN,2N3439
Q491	151-0219-00			SILICON,PNP,2N4250
Q514	151-0354-00			SILICON,PNP,QD400
Q515	151-0354-00			SILICON,PNP,QD400
Q542	151-0190-02			SILICON,NPN,2N3904
Q568	151-0150-00			SILICON,NPN,2N3440
Q569	151-0219-00			SILICON,PNP,2N4250
Q580	151-0169-00			SILICON,NPN,2N3439
Q624	151-0354-00			SILICON,PNP,QD400
Q625	151-0354-00			SILICON,PNP,QD400
Q1030	151-0286-00			SILICON,NPN,TEK SPEC
Q1032	151-0241-00			SILICON,NPN,TEK SPEC
Q1034	151-0241-00			SILICON,NPN,TEK SPEC
Q1036	151-0210-00			SILICON,NPN,TEK SPEC
Q1040	151-0349-00			SILICON,NPN,SJE924
Q1042	151-0373-00			SILICON,PNP,MJE2901
Q1044	151-0349-00			SILICON,NPN,SJE924
Q1046	151-0373-00			SILICON,PNP,MJE2901
RESISTORS				
R4	311-1136-00			100K OHM,VAR
R14	311-1328-00			100 OHM,VAR
R21	311-1136-00			100K OHM,VAR
R27	311-1136-00			100K OHM,VAR
R31	311-1328-00			100 OHM,VAR
R37	311-1136-00			100K OHM,VAR
R47	311-1287-00			100K OHM,VAR
R51	311-1288-00			200K OHM,VAR
R55	311-1287-00			100K OHM,VAR
R61	311-1288-00			200K OHM,VAR
R75	311-1133-00			10K OHM,VAR
R85	311-1133-00			10K OHM,VAR
R103	315-0680-00			68 OHM,0.25W,5%
R104	315-0680-00			68 OHM,0.25W,5%
R106	321-0385-00			100K OHM,0.125W,1%
R107	315-0511-00			510 OHM,0.25W,5%
R108	315-0101-00			100 OHM,0.25W,5%
R125A-H	307-0344-00			1.5 OHM,8 SECTION,FILM

DEFLECTION AMPL & STORAGE (cont)

Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Description
RESISTORS (cont)				
R136	315-0153-00			15K OHM,0.25W,5%
R137	315-0511-00			510 OHM,0.25W,5%
R142	307-0103-00			2.7 OHM,0.25W,5%
R143	315-0100-00			10 OHM,0.25W,5%
R145	321-0289-00			10K OHM,0.125W,1%
R152	321-0289-00			10K OHM,0.125W,1%
R153	321-0705-00			41.7K OHM,0.125W,1%
R155	315-0104-00			100K OHM,0.25W,5%
R156	321-0242-00			3.24K OHM,0.125W,1%
R157	321-0289-00			10K OHM,0.125W,1%
R158	321-0289-00			10K OHM,0.125W,1%
R159	321-0318-00			20K OHM,0.125W,1%
R169[1]	315-0101-03			100 OHM,0.25W,5%
R175	321-0324-00			23.2K OHM,0.125W,1%
R176	321-0306-00			15K OHM,0.125W,1%
R178	315-0682-00			6.8K OHM,0.25W,5%
R179	315-0222-00			2.2K OHM,0.25W,5%
R184	315-0104-00			100K OHM,0.25W,5%
R185	315-0102-00			1K OHM,0.25W,5%
R188	315-0202-00			2K OHM,0.25W,5%
R189	315-0104-00			100K OHM,0.25W,5%
R237	315-0101-00			100 OHM,0.25W,5%
R245	301-0242-00			2.4K OHM,0.50W,5%
R246	321-0324-00			23.2K OHM,0.125W,1%
R252	321-0289-00			10K OHM,0.125W,1%
R253	321-0289-00			10K OHM,0.125W,1%
R254	315-0512-00			5.1K OHM,0.25W,5%
R255	321-0289-00			10K OHM,0.125W,1%
R256	321-0289-00			10K OHM,0.125W,1%
R259	315-0103-00			10K OHM,0.25W,5%
R268	315-0102-00			1K OHM,0.25W,5%
R269	315-0201-00			200 OHM,0.25W,5%
R271	315-0101-00			100 OHM,0.25W,5%
R274	315-0392-00			3.9K OHM,0.25W,5%
R275	315-0432-00			4.3K OHM,0.25W,5%
R283	315-0103-00			10K OHM,0.25W,5%
R284	315-0203-00			20K OHM,0.25W,5%
R285	315-0203-00			20K OHM,0.25W,5%
R286	315-0103-00			10K OHM,0.25W,5%
R293	315-0103-00			10K OHM,0.25W,5%
R295	315-0182-00			1.8K OHM,0.25W,5%
R314	321-0289-00			10K OHM,0.125W,1%

[1] -00,-01,-02,-03 only.

DEFLECTION AMPL & STORAGE (cont)

Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Description
RESISTORS (cont)				
R315	315-0393-00			39K OHM,0.25W,5%
R316	321-0204-00			1.3K OHM,0.125W,1%
R318	303-0471-00			470 OHM,1W,5%
R328	303-0241-00			240 OHM,1W,5%
R332	321-0641-00			1.8K OHM,0.125W,1%
R333	315-0393-00			39K OHM,0.25W,5%
R334	321-0289-00			10K OHM,0.125W,1%
R335	321-0385-00			100K OHM,0.125W,1%
R342	307-0103-00			2.7 OHM,0.25W,5%
R343	315-0100-00			10 OHM,0.25W,5%
R353	321-0318-00			20K OHM,0.125W,1%
R354	315-0103-00			10K OHM,0.25W,5%
R355	321-0242-00			3.24K OHM,0.125W,1%
R356	315-0104-00			100K OHM,0.25W,5%
R357	321-0289-00			10K OHM,0.125W,1%
R358	321-0289-00			10K OHM,0.125W,1%
R359	321-0705-00			41.7K OHM,0.125W,1%
R369[1]	315-0472-00			4.7K OHM,0.25W,5%
R371	315-0472-00			4.7K OHM,0.25W,5%
R372	315-0101-00			100 OHM,0.25W,5%
R373	315-0102-00			1K OHM,0.25W,5%
R374	315-0182-00			1.8K OHM,0.25W,5%
R375	315-0133-00			13K OHM,0.25W,5%
R378	315-0102-00			1K OHM,0.25W,5%
R379	315-0182-00			1.8K OHM,0.25W,5%
R382	315-0133-00			13K OHM,0.25W,5%
R388	321-0260-00			4.99K OHM,0.125W,1%
R389	321-0307-00			15.4K OHM,0.125W,1%
R391	321-0274-00			6.98K OHM,0.125W,1%
R392	321-0260-00			4.99K OHM,0.125W,1%
R397	305-0104-00			100K OHM,2W,5%
R414	321-0289-00			10K OHM,0.25W,5%
R415	315-0470-00			47 OHM,0.25W,5%
R416	321-0304-00			14.3K OHM,0.125W,1%
R417	321-0289-00			10K OHM,0.125W,1%
R418	321-0289-00			10K OHM,0.125W,1%
R419	321-0304-00			14.3K OHM,0.125W,1%
R420	315-0753-00			75K OHM,0.25W,5%
R444	301-0242-00			2.4K OHM,0.50W,5%
R445	321-0324-00			23.2K OHM,0.125W,1%
R446	321-0289-00			10K OHM,0.125W,1%
R452	321-0289-00			10K OHM,0.125W,1%

[1] -00,-01,-02,-03 only.

DEFLECTION AMPL & STORAGE (cont)

Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Description
RESISTORS (cont)				
R453	315-0512-00			5.1K OHM,0.25W,5%
R454	321-0289-00			10K OHM,0.125W,1%
R455	321-0289-00			10K OHM,0.125W,1%
R458	321-0289-00			10K OHM,0.125W,1%
R459	321-0289-00			10K OHM,0.125W,1%
R467	315-0472-00			4.7K OHM,0.25W,5%
R470	315-0473-00			47K OHM,0.25W,5%
R475	315-0682-00			6.8K OHM,0.25W,5%
R479	301-0474-00			470K OHM,0.50W,5%
R481	315-0101-00			100 OHM,0.25W,5%
R485	305-0683-00			68K OHM,2W,5%
R486	315-0101-00			100 OHM,0.25W,5%
R488	321-0363-00			59K OHM,0.125W,1%
R489	315-0682-00			6.8K OHM,0.25W,5%
R492	315-0101-00			100 OHM,0.25W,5%
R519	321-0289-00			10K OHM,0.125W,1%
R520	321-0289-00			10K OHM,0.125W,1%
R521	321-0304-00			14.3K OHM,0.125W,1%
R522	321-0289-00			10K OHM,0.25W,5%
R523	321-0289-00			10K OHM,0.25W,5%
R524	321-0304-00			14.3K OHM,0.125W,1%
R528	315-0753-00			75K OHM,0.25W,5%
R529	315-0470-00			47 OHM,0.25W,5%
R531	321-0289-00			10K OHM,0.125W,1%
R532	321-0289-00			10K OHM,0.125W,1%
R533	321-0318-00			20K OHM,0.125W,1%
R534	321-0314-00	B010100	B010104	18.2K OHM,0.125W,1%
R534	321-0318-00	B010105		20K OHM,0.125W,1%
R535	321-0318-00			20K OHM,0.125W,1%
R536	315-0753-00			75K OHM,0.25W,5%
R537	321-0289-00			10K OHM,0.125W,1%
R545	315-0303-00			30K OHM,0.25W,5%
R546	315-0303-00			30K OHM,0.25W,5%
R547	315-0153-00			15K OHM,0.25W,5%
R548	315-0472-00			4.7K OHM,0.25W,5%
R549[1]	315-0822-00			8.2K OHM,0.25W,5%
R555[2]	315-0102-00			1K OHM,0.25W,5%
R556	315-0472-00			4.7K OHM,0.25W,5%
R559	321-0251-00			4.02K OHM,0.125W,1%
R562	315-0393-00			39K OHM,0.25W,5%
R563	315-0102-00			1K OHM,0.25W,5%
R564	315-0182-00			1.8K OHM,0.25W,5%
R565	315-0133-00			13K OHM,0.25W,5%
R566	315-0473-00			47K OHM,0.25W,5%

[1]-00,-01,-02,-03 only.
[2]-04 only.

DEFLECTION AMPL & STORAGE (cont)

Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Description
RESISTORS (cont)				
R567	315-0223-00			22K OHM,0.25W,5%
R574	305-0104-00			100K OHM,2W,5%
R575	315-0101-00			100 OHM,0.25W,5%
R588	323-0398-00			137K OHM,0.50W,1%
R590	315-0101-00			100 OHM,0.25W,5%
R593	315-0101-00			100 OHM,0.25W,5%
R594	306-0124-00			120K OHM,2W,10%
R614	321-0289-00	B010100	B010104	10K OHM,0.125W,1%
R614	321-0301-00	B010105		13.3K OHM,0.125W,1%
R615	315-0470-00			47 OHM,0.25W,5%
R616	321-0277-00			7.5K OHM,0.125W,1%
R617	321-0261-00			5.11K OHM,0.125W,1%
R630	321-0261-00			5.11K OHM,0.125W,1%
R631	321-0277-00			7.5K OHM,0.125W,1%
R632	315-0470-00			47 OHM,0.25W,5%
R633	321-0289-00			10K OHM,0.125W,1%
R634	321-0289-00			10K OHM,0.125W,1%
R635	321-0318-00	B010100	B010104	20K OHM,0.125W,1%
R635	321-0306-00	B010105		15K OHM,0.125W,1%
R636	321-0314-00	B010100	B010104	18.2K OHM,0.125W,1%
R636	321-0289-00	B010105		10K OHM,0.125W,1%
R637	321-0318-00			20K OHM,0.125W,1%
R638	315-0753-00			75K OHM,0.25W,5%
R639	321-0289-00			10K OHM,0.125W,1%
R647[1]	315-0103-00			10K OHM,0.25W,5%
R647[2]	315-0102-00			1K OHM,0.25W,5%
R648[2]	315-0102-00			1K OHM,0.25W,5%
R654[1]	315-0101-03			100 OHM,0.25W,5%
R655	315-0472-00			4.7K OHM,0.25W,5%
R665	307-0103-00			2.7 OHM,0.25W,5%
R670	307-0103-00			2.7 OHM,0.25W,5%
R674	301-0100-00			10 OHM,0.50W,5%
R675	301-0100-00			10 OHM,0.50W,5%
R678	315-0101-00			100 OHM,0.25W,5%
R683	303-0224-00			220K OHM,1W,5%
R684	323-0452-00			499K OHM,0.50W,1%
R686	315-0101-00			100 OHM,0.25W,5%
R688	315-0470-00			47 OHM,0.25W,5%
R689	315-0470-00			47 OHM,0.25W,5%
R691	315-0104-00			100K OHM,0.25W,5%
INTEGRATED CIRCUITS				
U149	156-0067-07			OPERATIONAL AMPLIFIER,UA741C
U165	156-0093-00			HEX. INVERTER,SN7416N
U249	156-0067-07			OPERATIONAL AMPLIFIER,UA741C
U265	156-0043-00			QUAD 2-INPUT POSITIVE NOR GATE,SN7402N

[1]-00,-01,-02,-03 only.
[2]-04 only.

Ⓑ

DEFLECTION AMPL & STORAGE (cont)

Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Description
INTEGRATED CIRCUITS (cont)				
U349	156-0067-07			OPERATIONAL AMPLIFIER,UA741C
U425	156-0067-07			OPERATIONAL AMPLIFIER,UA741C
U426	156-0067-07			OPERATIONAL AMPLIFIER,UA741C
U449	156-0067-07			OPERATIONAL AMPLIFIER,UA741C
U465	156-0172-00			DUAL RETRIGGERABLE MONOSTABLE MULTI-VIBRATOR,SN74123N
U525	155-0035-00			MONOLITHIC,QUAD OPERATIONAL AMPLIFIER
U538	155-0035-00			MONOLITHIC,QUAD OPERATIONAL AMPLIFIER
U555[1]	156-0172-00			DUAL RETRIGGERABLE MONOSTABLE MULTI-VIBRATOR,SN74123N
U555[2]	156-0149-00			DUAL 4-INPUT POS. NAND GATED SCHMITT TRIGGER,SN7413N
U649	156-0030-00			QUAD 2-INPUT POSITIVE NAND GATE
U657	156-0145-00			QUAD 2-INPUT POSITIVE NAND BUFFER,SN7438N
DIODES,ZENER				
VR135	152-0279-00			1N751A,0.4W,5.1V,5%
VR398	152-0087-00			1N3044B,1W,100V,5%
VR476	152-0059-00			1N9625,1W,12.6V,5%
VR694	152-0298-00			1N3814B,1.5W,110V,5%

A6 ASSEMBLY HV & Z AXIS

Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Description
ASSEMBLIES				
A6	670-2521-00	B010100	B019999	CIRCUIT BOARD ASSEMBLY, HV & Z AXIS
A6	670-2521-01	B020000		CIRCUIT BOARD ASSEMBLY, HV & Z AXIS
CAPACITORS				
C15	283-0034-00			0.005UF,CER,4000V
C16	283-0034-00			0.005UF,CER,4000V
C64	283-0101-00			4700PF,CER,6000V,+80-20%
C65	283-0101-00			4700PF,CER,6000V,+80-20%
C79	283-0057-00	B010100	B019999	0.1UF,CER,200V,+80-20%
C79	283-0008-00	B020000		0.1UF,CER,500V
C82	283-0002-00			0.01UF,CER,500V
C83	283-0057-00	B010100	B019999	0.1UF,CER,200V,+80-20%
C83	283-0008-00	B020000		0.1UF,CER,500V
C95	283-0008-00			0.1UF,CER,500V
C135	283-0291-00			25PF,CER,6000V,10%
C138	283-0101-00			4700PF,CER,6000V,+80-20%
C143	283-0101-00			4700PF,CER,6000V,+80-20%
C145	283-0101-00			4700PF,CER,6000V,+80-20%
C149	283-0101-00			4700PF,CER,6000V,+80-20%
C174	290-0527-00			15UF,ELECT.,20V,20%
C181	281-0580-00			470PF,CER,500V,10%
C183	290-0534-00			1UF,ELECT.,35V,20%
C196	281-0500-00			2.2PF,CER,500V,±0.5PF
C209	283-0177-00			1UF,CER,25V,+80-20%

[1]-00,-01,-02,-03 only.
[2]-04 only.

HV & Z AXIS (cont)

Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Description
CAPACITORS (cont)				
C214	283-0067-00			0.001UF,CER,200V,10%
C246	283-0002-00			0.01UF,CER,500V
C255	283-0101-00			4700PF,CER,6000V,+80-20%
C268	283-0002-00			0.01UF,CER,500V
C289	283-0067-00			0.001UF,CER,200V,10%
C294	281-0504-00			10PF,CER,500V,10%
C315	290-0559-00			22UF,ELECT.,35V,20%
C336	283-0067-00			0.001UF,CER,200V,10%
C339	290-0534-00			1UF,ELECT.,35V,20%
C341	290-0534-00			1UF,ELECT.,35V,20%
C362	281-0510-00			22PF,CER,500V,20%
C363	281-0547-00			2.7PF,CER,500V,10%
C364	281-0541-00			6.8PF,CER,500V,10%
C373	290-0534-00			1UF,ELECT.,35V,20%
C375	290-0534-00			1UF,ELECT.,35V,20%
C397	283-0002-00			0.01UF,CER,500V
DIODES,SILICON				
CR1	152-0408-00			VF5-12X
CR5	152-0408-00			VF5-12X
CR21	152-0408-00			VF5-12X
CR25	152-0408-00			VF5-12X
CR45	152-0242-00			CD12691
CR53	152-0242-00			CD12691
CR72	152-0061-00			CD8393 or FDH2161
CR73	152-0061-00			CD8393 or FDH2161
CR74	152-0061-00			CD8393 or FDH2161
CR75	152-0061-00			CD8393 or FDH2161
CR79	152-0061-00			CD8393 or FDH2161
CR81	152-0061-00			CD8393 or FDH2161
CR87	152-0141-02			1N4152
CR177	152-0061-00			CD8393 or FDH2161
CR178	152-0061-00			CD8393 or FDH2161
CR189	152-0141-02			1N4152
CR198	152-0141-02			1N4152
CR201	152-0412-00			SR1936
CR249	152-0066-00			DIFFUSED,SELECTED FROM 1N3194
CR273	152-0333-00			FDH6012
CR286	152-0141-02			1N4152
CR311	152-0333-00			FDH6012
CR332	152-0141-02			1N4152
CR334	152-0141-02			1N4152
CR349	152-0066-00			DIFFUSED,SELECTED FROM 1N3194
CR361	152-0333-00			FDH6012

HV & Z AXIS (cont)

Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Description
DIODES,SILICON (cont)				
CR362	152-0141-02			1N4152
CR367	152-0141-02			1N4152
BULBS				
DS32	150-0035-00			NEON,A1D-T
DS33	150-0035-00			NEON,A1D-T
DS34	150-0035-00			NEON,A1D-T
DS41	150-0035-00			NEON,A1D-T
DS48	150-0035-00			NEON,A1D-T
DS51	150-0035-00			NEON,A1D-T
DS53	150-0035-00			NEON,A1D-T
DS55	150-0035-00			NEON,A1D-T
DS74	150-0035-00			NEON,A1D-T
DS173	150-0035-00			NEON,A1D-T
DS244	150-0035-00			NEON,A1D-T
DS246	150-0035-00			NEON,A1D-T
DS249	150-0035-00			NEON,A1D-T
DS257	150-0035-00			NEON,A1D-T
DS258	150-0035-00			NEON,A1D-T
DS259	150-0035-00			NEON,A1D-T
INDUCTORS				
L173	108-0213-00			2.5MH
L311	108-0234-00			130UH
L318	108-0422-00			80UH
TRANSISTORS				
Q91	151-0279-00			SILICON,NPN,SE7056
Q175	151-0124-00			SILICON,NPN,SELECTED FROM 2N3501
Q185	151-0279-00			SILICON,NPN,SE7056
Q187	151-0270-00			SILICON,PNP,SELECTED FROM 2N3495
Q196	151-0190-02			SILICON,NPN,2N3904
Q197	151-0311-01			SILICON,NPN,MJE340
Q274	151-0279-00			SILICON,NPN,SE7056
Q282	151-0279-00			SILICON,NPN,SE7056
Q301	151-0256-00			SILICON,PNP,SELECTED FROM DTS411
Q323	151-0334-00			SILICON,NPN,MJE520
Q329	151-0302-00			SILICON,NPN,2N2222A
Q333	151-1005-00			SILICON,FET,N CHANNEL,TEK SPEC
Q357	151-0169-00			SILICON,NPN,2N3439
Q358	151-0169-00			SILICON,NPN,2N3439
Q378	151-1004-00			SILICON,FET,N CHANNEL,KE4220 or EQUIVALENT
Q379	151-0302-00			SILICON,NPN,2N2222A
Q383	151-0302-00			SILICON,NPN,2N2222A
Q389	151-1004-00			SILICON,FET,N CHANNEL,KE4220 or EQUIVALENT
Q391	151-0302-00			SILICON,NPN,2N2222A

HV & Z AXIS (cont)

Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Description
RESISTORS				
R38	301-0101-00			100 OHM,0.50W,5%
R40	301-0101-00			100 OHM,0.50W,5%
R41	301-0273-00			27K OHM,0.50W,5%
R45	301-0104-00			100K OHM,0.50W,5%
R47	315-0102-00			1K OHM,0.25W,5%
R52	301-0395-00			3.9M OHM,0.50W,5%
R55	315-0102-00			1K OHM,0.25W,5%
R73	315-0202-00			2K OHM,0.25W,5%
R77	305-0185-00	B010100	B010182	1.8M OHM,2W,5%
R77	305-0125-00	B010183		1.2M OHM,2W,5%
R82	315-0100-00			10 OHM,0.25W,5%
R83	315-0472-00			4.7K OHM,0.25W,5%
R85	321-0306-00			15K OHM,0.125W,1%
R86	311-1235-00			100K OHM,VAR
R87	315-0472-00			4.7K OHM,0.25W,5%
R91	311-1235-00			100K OHM,VAR
R92	315-0101-00			100 OHM,0.25W,5%
R94	315-0103-00			10K OHM,0.25W,5%
R97	301-0104-00			100K OHM,0.50W,5%
R98	301-0222-00			2.2K OHM,0.50W,5%
R161	311-1323-00			5M OHM,VAR
R174	315-0101-00			100 OHM,0.25W,5%
R175	301-0393-00			39K OHM,0.50W,5%
R178	315-0100-00			10 OHM,0.25W,5%
R179	315-0301-00			300 OHM,0.25W,5%
R181	315-0471-00			470 OHM,0.25W,5%
R183	315-0132-00			1.3K OHM,0.25W,5%
R185	315-0220-00			22 OHM,0.25W,5%
R186	315-0471-00			470 OHM,0.25W,5%
R187	315-0102-00			1K OHM,0.25W,5%
R188	315-0153-00			15K OHM,0.25W,5%
R191	303-0513-00			51K OHM,1W,5%
R192	315-0104-00			100K OHM,0.25W,5%
R193	321-0269-00			6.19K OHM,0.125W,1%
R194	321-0289-00			10K OHM,0.125W,1%
R195	321-0411-00			187K OHM,0.125W,1%
R196	321-0406-00			165K OHM,0.125W,1%
R197	321-0371-00			71.5K OHM,0.125W,1%
R202	315-0103-00			10K OHM,0.25W,5%
R227	311-1232-00			50K OHM,VAR
R231	315-0104-00			100K OHM,0.25W,5%
R233	321-0423-00			249K OHM,0.125W,1%
R236	315-0224-00			220K OHM,0.25W,5%

HV & Z AXIS (cont)

Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Description
RESISTORS (cont)				
R238	315-0824-00			820K OHM,0.25W,5%
R241A,B	307-0314-00			228K OHM/60M OHM,THICK FILM
R251	315-0333-00			33K OHM,0.25W,5%
R253A,B	307-0316-00			26.8M OHM/15M OHM,THICK FILM
R261	315-0222-00			2.2K OHM,0.25W,5%
R269	315-0470-00			47 OHM,0.25W,5%
R271	308-0108-00			15K OHM,5W,WW,5%
R272	315-0100-00			10 OHM,0.25W,5%
R273	321-0241-00			3.16K OHM,0.125W,1%
R274	315-0303-00			30K OHM,0.25W,5%
R275	315-0623-00			62K OHM,0.25W,5%
R276	315-0334-00			330K OHM,0.25W,5%
R277	307-0103-00			2.7 OHM,0.25W,5%
R278	315-0221-00			220 OHM,0.25W,5%
R279	321-0330-00			26.7K OHM,0.125W,1%
R280	315-0301-00			300 OHM,0.25W,5%
R281	315-0102-00			1K OHM,0.25W,5%
R282	321-0255-00			4.42K OHM,0.125W,1%
R283	315-0561-00			560 OHM,0.25W,5%
R284	315-0152-00			1.5K OHM,0.25W,5%
R285	315-0303-00			30K OHM,0.25W,5%
R286	315-0623-00			62K OHM,0.25W,5%
R287	315-0102-00			1K OHM,0.25W,5%
R288	315-0334-00			330K OHM,0.25W,5%
R289	315-0472-00			4.7K OHM,0.25W,5%
R290	305-0473-00			47K OHM,2W,5%
R293	321-0280-00			8.06K OHM,0.125W,1%
R294	315-0335-00			3.3M OHM,0.25W,5%
R295	315-0123-00			12K OHM,0.25W,5%
R297	321-0274-00			6.98K OHM,0.125W,1%
R298	305-0393-00			39K OHM,2W,5%
R310	308-0244-00			0.3 OHM,2W,WW,10%
R317	301-0272-00			2.7K OHM,0.50W,5%
R325	315-0221-00			220 OHM,0.25W,5%
R327	304-0152-00			1.5K OHM,1W,10%
R329	315-0103-00			10K OHM,0.25W,5%
R330	315-0272-00			2.7K OHM,0.25W,5%
R338	315-0100-00			10 OHM,0.25W,5%
R342	315-0100-00			10 OHM,0.25W,5%
R346	315-0102-00			1K OHM,0.25W,5%
R351	305-0104-00			100K OHM,2W,5%
R355	315-0103-00			10K OHM,0.25W,5%
R364	315-0472-00			4.7K OHM,0.25W,5%

HV & Z AXIS (cont)

Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Description
RESISTORS (cont)				
R366	321-0452-00			499K OHM,0.125W,1%
R368	315-0335-00			3.3M OHM,0.25W,5%
R371	321-0306-00			15K OHM,0.125W,1%
R372	315-0220-00			22 OHM,0.25W,5%
R379	321-0280-00			8.06K OHM,0.125W,1%
R381	315-0102-00			1K OHM,0.25W,5%
R382	311-1235-00			100K OHM,VAR
R386	321-0289-00			10K OHM,0.125W,1%
R387	321-0306-00			15K OHM,0.125W,1%
R389	311-1235-00			100K OHM,VAR
R394	315-0242-00			2.4K OHM,0.25W,5%
R395	315-0472-00			4.7K OHM,0.25W,5%
R397	315-0220-00			22 OHM,0.25W,5%
TRANSFORMER				
T101	120-0826-00			HV POWER
INTEGRATED CIRCUITS				
U295	156-0067-07			OPERATIONAL AMPLIFIER,UA741C
U375	156-0067-07			OPERATIONAL AMPLIFIER,UA741C

A7 ASSEMBLY LV POWER SUPPLY

Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Description
ASSEMBLIES				
A7	670-1726-01	B010100	B029999	CIRCUIT BOARD ASSEMBLY, LV POWER SUPPLY
A7	670-1726-02	B030000		CIRCUIT BOARD ASSEMBLY, LV POWER SUPPLY
CAPACITORS				
C9A,	290-0549-00			150UF,ELECT.,400V,+50-10%
B				150UF,ELECT.,200V,+75-10%
C23	290-0568-00			4500UF,ELECT.,25V,+75-10%
C29	290-0534-00			1UF,ELECT.,35V,20%
C31	283-0000-00			0.001UF,CER,500V,+100-10%
C34	281-0525-00			470PF,CER,500V,20%
C35	283-0057-00			0.1UF,CER,200V,+80-20%
C39	290-0536-00			10UF,ELECT.,25V,20%
C42	290-0536-00			10UF,ELECT.,25V,20%
C43	290-0534-00			1UF,ELECT.,35V,20%
C44	283-0000-00			0.001UF,CER,500V,+100-0%
C45	281-0525-00			470PF,CER,500V,20%
C46	283-0028-00			0.0022UF,CER,50V
C50	281-0546-00			330PF,CER,500V,10%
C53	290-0568-00			4500UF,ELECT.,25V,+75-10%
C58	283-0000-00			0.001UF,CER,500V,+100-10%
C59	281-0525-00			470PF,CER,500V,20%
C61	283-0000-00			0.001UF,CER,500V,+100-0%

LV POWER SUPPLY (cont)

Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Description
CAPACITORS (cont)				
C62	281-0523-00			100PF,CER,350V,20%
C66	290-0536-00			10UF,ELECT.,25V,20%
C119	283-0067-00	XB030000		0.001UF,CER,200V,10%
DIODES,SILICON				
CR13	152-0200-00			SBR4
CR21	152-0066-00			DIFFUSED,SELECTED FROM 1N3194
CR23	152-0462-00			MDA960-3
CR53	152-0462-00			MDS960-3
CR55	152-0066-00			DIFFUSED,SELECTED FROM 1N3194
CR58	152-0233-00			CD61128
CR61	152-0066-00			DIFFUSED,SELECTED FROM 1N3194
FUSES				
F21	159-0021-00			CARTRIDGE,2A,3AG,FAST-BLO
F41	159-0013-00			CARTRIDGE,6A,3AG,FAST-BLO
F61	159-0021-00			CARTRIDGE,2A,3AG,FAST-BLO
TRANSISTORS				
Q29	151-0302-00			SILICON,NPN,2N2222A
Q73	151-0134-00			SILICON,PNP,2N2905A
Q75	151-0331-00			SILICON,NPN,D40C8
Q97	151-0515-01			SILICON,SCR,PNP,8A,50V,2N4441
Q99	151-0188-00			SILICON,PNP,2N3906
Q117	151-0337-00			SILICON,NPN,2N3055
Q119	151-0302-00			SILICON,NPN,2N2222A
RESISTORS				
R7	303-0623-00			62K OHM,1W,5%
R9	304-0184-00			180K OHM,1W,10%
R23	303-0182-00			1.8K OHM,1W,5%
R25	305-0273-00	B010100	B029999	27K OHM,2W,5%
R25	322-0197-00	B030000		1.1K OHM,0.125W,1%
R26	321-0181-00			750 OHM,0.125W,1%
R27	311-1225-00			1K OHM,VAR
R28	321-0262-00	B010100	B029999	5.23K OHM,0.125W,1%
R28	321-0251-00	B030000		4.02K OHM,0.125W,1%
R29	315-0103-00			10K OHM,0.25W,5%
R30	315-0204-00	B010100	B029999X	200K OHM,0.25W,5%
R31	321-0271-00			6.49K OHM,0.125W,1%
R32	321-0242-00			3.24K OHM,0.125W,1%
R34	315-0205-00			2M OHM,0.25W,5%
R35	315-0102-00			1K OHM,0.25W,5%
R36	315-0103-00			10K OHM,0.25W,5%
R37	305-0823-00			82K OHM,2W,5%
R43	315-0103-00			10K OHM,0.25W,5%

LV POWER SUPPLY (cont)

Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Description
RESISTORS (cont)				
R44	315-0102-00			1K OHM,0.25W,5%
R45	315-0205-00			2M OHM,0.25W,5%
R46	315-0103-00			10K OHM,0.25W,5%
R47	315-0472-00			4.7K OHM,0.25W,5%
R48	315-0472-00			4.7K OHM,0.25W,5%
R50	311-1228-00			10K OHM,VAR
R51	315-0470-00			47 OHM,0.25W,5%
R52	315-0102-00			1K OHM,0.25W,5%
R53	303-0182-00			1.8K OHM,1W,5%
R57	321-0289-00			10K OHM,0.125W,1%
R58	321-0289-00			10K OHM,0.125W,1%
R59	315-0205-00			2M OHM,0.25W,5%
R61	315-0273-00			27K OHM,0.25W,5%
R63	301-0151-00			150 OHM,0.50W,5%
R64	315-0472-00			4.7K OHM,0.25W,5%
INTEGRATED CIRCUITS				
U69	156-0067-00			OPERATIONAL AMPLIFIER,UA741C
U71	156-0067-00			OPERATIONAL AMPLIFIER,UA741C
U77	156-0067-00			OPERATIONAL AMPLIFIER,UA741C
DIODES,ZENER				
VR25	152-0461-00			1N821,0.4W,6.2V,5%
VR35	152-0279-00			1N751A,0.4W,5.1V,5%
VR47	152-0279-00			1N751A,0.4W,5.1V,5%
VR119	152-0283-00			1N976B,0.4W,43V,5%

A8 ASSEMBLY KEYBOARD

Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Description
ASSEMBLY				
A8	119-0374-00			KEYBOARD ASSEMBLY
CAPACITORS				
C1	290-0536-00			10UF,ELECT.,25V,20%
C2	283-0239-00			0.022UF,CER,100V,10%
C3	290-0534-00			1UF,ELECT.,35V,20%
C4	283-0239-00			0.022UF,CER,100V,10%
C5	290-0301-00			10UF,ELECT.,20V,10%
C6	290-0488-00			2.2UF,ELECT.,20V,10%
C7	290-0536-00			10UF,ELECT.,25V,20%
C8 THRU C11	283-0003-00			0.01UF,CER,150V,+80-20%
BULB				
DS1	150-0093-01			INCANDESCENT,5V,60MA,SELECTED

KEYBOARD (cont)

Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Description
TRANSISTORS				
Q1	151-0188-00			SILICON,PNP,2N3906
Q2	151-0302-00			SILICON,NPN,2N2222A
Q3	151-0188-00			SILICON,PNP,2N3906
Q4	151-0302-00			SILICON,NPN,2N2222A
Q5	151-0302-00			SILICON,NPN,2N2222A
RESISTORS				
R1	315-0202-00			2K OHM,0.25W,5%
R2	315-0202-00			2K OHM,0.25W,5%
R3	315-0202-00			2K OHM,0.25W,5%
R4	315-0333-00			33K OHM,0.25W,5%
R5	315-0331-00			330 OHM,0.25W,5%
R6	315-0202-00			2K OHM,0.25W,5%
R9	315-0470-00			47 OHM,0.25W,5%
R10	315-0202-00			2K OHM,0.25W,5%
R11	315-0202-00			2K OHM,0.25W,5%
R12	315-0623-00			62K OHM,0.25W,5%
R13	315-0511-00			510 OHM,0.25W,5%
R14	315-0103-00			10K OHM,0.25W,5%
R15	315-0103-00			10K OHM,0.25W,5%
R16	315-0223-00			22K OHM,0.25W,5%
R17	315-0103-00			10K OHM,0.25W,5%
R18	315-0511-00			510 OHM,0.25W,5%
R19	315-0202-00			2K OHM,0.25W,5%
R20	315-0103-00			10K OHM,0.25W,5%
R21	315-0103-00			10K OHM,0.25W,5%
R22	315-0202-00			2K OHM,0.25W,5%
R23	315-0202-00			2K OHM,0.25W,5%
R24	315-0100-00			10 OHM,0.25W,5%
SWITCHES				
S1 THRU S60	260-1507-00			REED
INTEGRATED CIRCUITS				
Z1	156-0041-00			DUAL 15MHZ D-TYPE POS.-EDGE-TRIG. FLIP-FLOP, SN7474N
Z2	156-0075-00			SINGLE 8-BIT DATA SELECTOR/MULTIPLEXER, SN74151N
Z3	156-0041-00			DUAL 15MHZ D-TYPE POS.-EDGE-TRIG. FLIP-FLOP, SN7474N
Z4	156-0075-00			SINGLE 8-BIT DATA SELECTOR/MULTIPLEXER, SN74151N
Z5	156-0032-00			SINGLE 10MHZ 1-&-3-BIT BINARY RIPPLE COUNTER,SN7493N

KEYBOARD (cont)

Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Description
INTEGRATED CIRCUITS (cont)				
Z6	156-0111-00			SINGLE BCD-TO-DECIMAL DECODER/DRIVER, SN74145N
Z7	156-0047-00			TRIPLE 3-INPUT POSITIVE NAND GATE,SN7410N
Z8	156-0030-00			QUAD 2-INPUT POSITIVE NAND GATE,SN7400N
Z9	156-0058-00			HEX. INVERTER,SN7404N
Z10	156-0149-00			DUAL 4-INPUT POS. NAND GATED SCHMITT TRIGGER,SN7413N
Z11	156-0035-00			SINGLE 8-INPUT POSITIVE NAND GATE,SN7430N
Z12	156-0030-00			QUAD 2-INPUT POSITIVE NAND GATE,SN7400N
Z13	156-0034-00			DUAL 4-INPUT POSITIVE NAND GATE,SN7420N
Z14	156-0062-00			QUAD 2-INPUT POSITIVE EXCLUSIVE-OR GATE, SN7486N
Z15	156-0034-00			DUAL 4-INPUT POSITIVE NAND GATE,SN7420N
Z16	156-0041-00			DUAL 15MHZ D-TYPE POS.-EDGE-TRIG. FLIP-FLOP, SN7474N
Z17	156-0043-00			QUAD 2-INPUT POSITIVE NOR GATE,SN7402N
Z18	156-0041-00			DUAL 15MHZ D-TYPE POS.-EDGE-TRIG. FLIP-FLOP, SN7474N
Z19	156-0043-00			QUAD 2-INPUT POSITIVE NOR GATE,SN7402N
Z20	156-0145-00			QUAD 2-INPUT POSITIVE NAND BUFFER,SN7438N
Z21	156-0149-00			DUAL 4-INPUT POS. NAND GATED SCHMITT TRIGGER,SN7413N
Z22	156-0092-00			HEX. INVERTER,SN7405N

A9 ASSEMBLY HARD COPY

Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Description
ASSEMBLY				
A9	670-2570-00			CIRCUIT BOARD ASSEMBLY, HARD COPY
CAPACITORS				
C65	281-0623-00			650PF,CER,500V,5%
C67	281-0623-00			650PF,CER,500V,5%
C75	281-0512-00			27PF,CER,500V,10%
C85	281-0623-00			650PF,CER,500V,5%
C95	283-0178-00			0.1UF,CER,100V,+80-20%
C129	283-0194-00			4.7UF,CER,50V,20%
C131	283-0194-00			4.7UF,CER,50V,20%
C179	283-0000-00			0.001UF,CER,500V,+100-0%
C185	281-0623-00			650PF,CER,500V,5%
C195	283-0178-00			0.1UF,CER,100V,+80-20%
C231	283-0008-00			0.1UF,CER,500V
C235	283-0008-00			0.1UF,CER,500V
C245	290-0285-00			4UF,ELECT.,200V,+50-10%
C265	290-0536-00			10UF,CER,25V,20%

HARD COPY (cont)

Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Description
CAPACITORS (cont)				
C275	283-0178-00			0.1UF,CER,100V,+80-20%
C279	290-0536-00			10UF,ELECT.,25V,20%
C281	283-0178-00			0.1UF,CER,100V,+80-20%
C289	290-0536-00			10UF,ELECT.,25V,20%
C291	281-0523-00			100PF,CER,350V,20%
DIODES,SILICON				
CR105	152-0107-00			TI60 OR 1N647
CR121	152-0040-00			1N2615
CR145	152-0426-00			RECTIFIER,400V,0.4A,SELECTED FROM 1N647
CONNECTORS				
J119	131-1233-00			TERMINAL,PIN
J129	136-0058-00			SOCKET,7 PIN
J159	131-0589-00			TERMINAL,PIN
INDUCTORS				
L9	108-0422-00			80UH
L19	108-0422-00			80UH
L45	108-0146-00			5UH
L229	108-0324-00			10MH
L238	108-0324-00			10MH
L251	108-0324-00			10MH
TRANSISTOR				
Q275	151-0134-00			SILICON,PNP,2N2905A
RESISTORS				
R45	315-0681-00			680 OHM,0.25W,5%
R65	315-0102-00			1K OHM,0.25W,5%
R67	315-0103-00			10K OHM,0.25W,5%
R75	315-0103-00			10K OHM,0.25W,5%
R95	315-0100-00			10 OHM,0.25W,5%
R135	315-0103-00			10K OHM,0.25W,5%
R137	315-0101-00			100 OHM,0.25W,5%
R138	315-0101-00			100 OHM,0.25W,5%
R139	315-0101-00			100 OHM,0.25W,5%
R149	301-0104-00			100K OHM,0.50W,5%
R165	315-0102-00			1K OHM,0.25W,5%
R166	315-0103-00			10K OHM,0.25W,5%
R167	311-1228-00			10K OHM,VAR
R175	315-0513-00			51K OHM,0.25W,5%
R177	315-0153-00			15K OHM,0.25W,5%
R179	315-0432-00			4.3K OHM,0.25W,5%
R185	315-0103-00			10K OHM,0.25W,5%
R189	315-0100-00			10 OHM,0.25W,5%
R195	307-0103-00			2.7 OHM,0.25W,5%

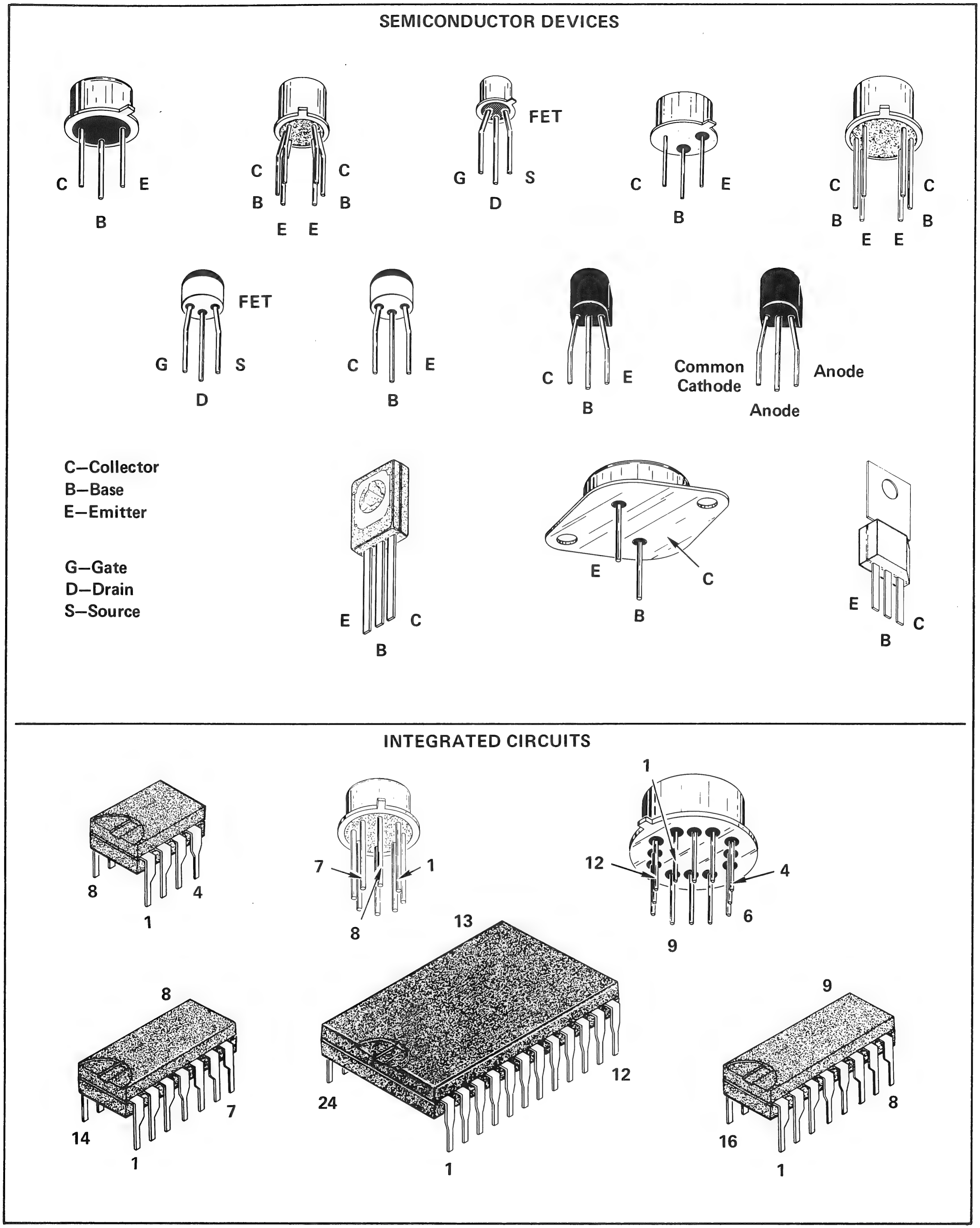
HARD COPY (cont)

Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Description
RESISTORS (cont)				
R265	311-1251-00			200K OHM,VAR
R267	307-0103-00			2.7 OHM,0.25W,5%
R269	321-0214-00			1.65K OHM,0.125W,1%
R275	301-0151-00			150 OHM,0.50W,5%
R277	321-0231-00			2.49K OHM,0.125W,1%
R278	307-0103-00			2.7 OHM,0.25W,5%
R281	315-0472-00			4.7K OHM,0.25W,5%
R285	315-0472-00			4.7K OHM,0.25W,5%
R295	315-0102-00			1K OHM,0.25W,5%
R297	315-0562-00			5.6K OHM,0.25W,5%
TRANSFORMER				
T38	120-0827-00			TOROID,THREE 12 TURN WINDINGS
INTEGRATED CIRCUITS				
U59	156-0162-00			SINGLE VIDEO AMPLIFIER,UA733C
U79	156-0162-00			SINGLE VIDEO AMPLIFIER,UA733C
U95	156-0096-00			VOLTAGE COMPARATOR,LM311
U289	156-0072-00			SINGLE MONOSTABLE MULTIVIBRATOR-ONE SHOT-,SN74121N

CIRCUITS

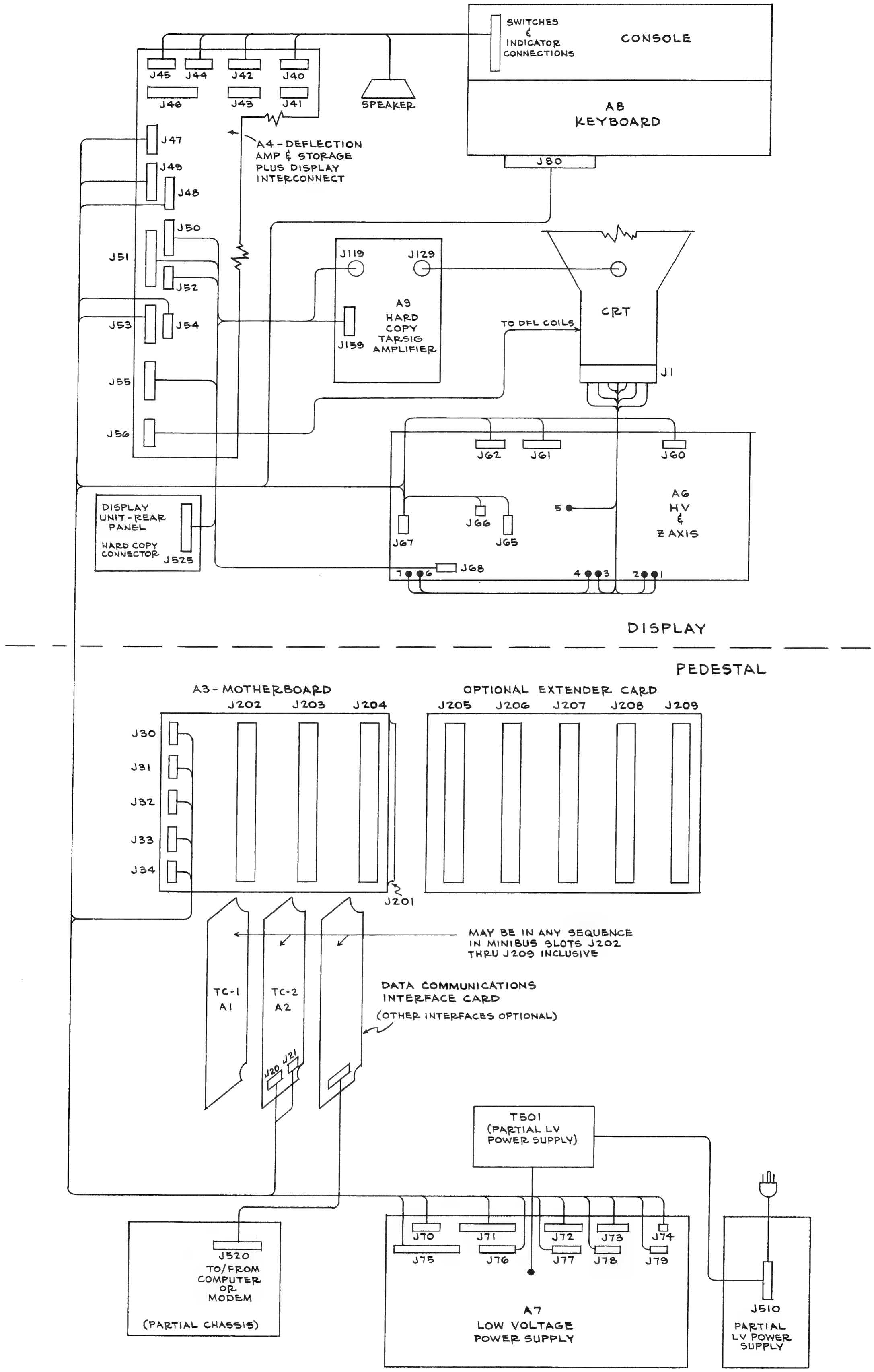
CONTENTS

CONTENTS



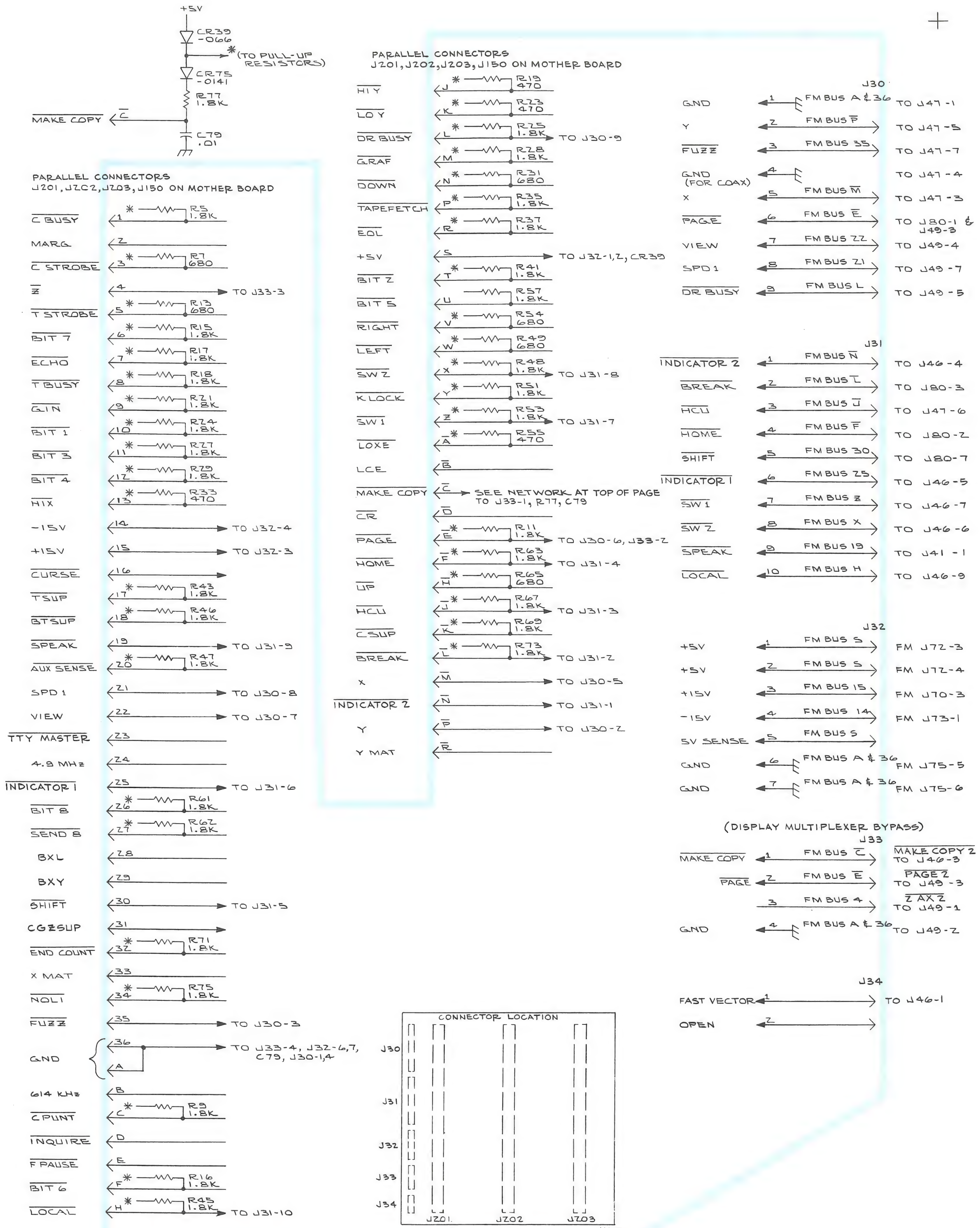
Ⓐ

Fig. 6-1. Semiconductor Information.



4012

FIG 6-2 CONNECTORS & WIRING DIAGRAM

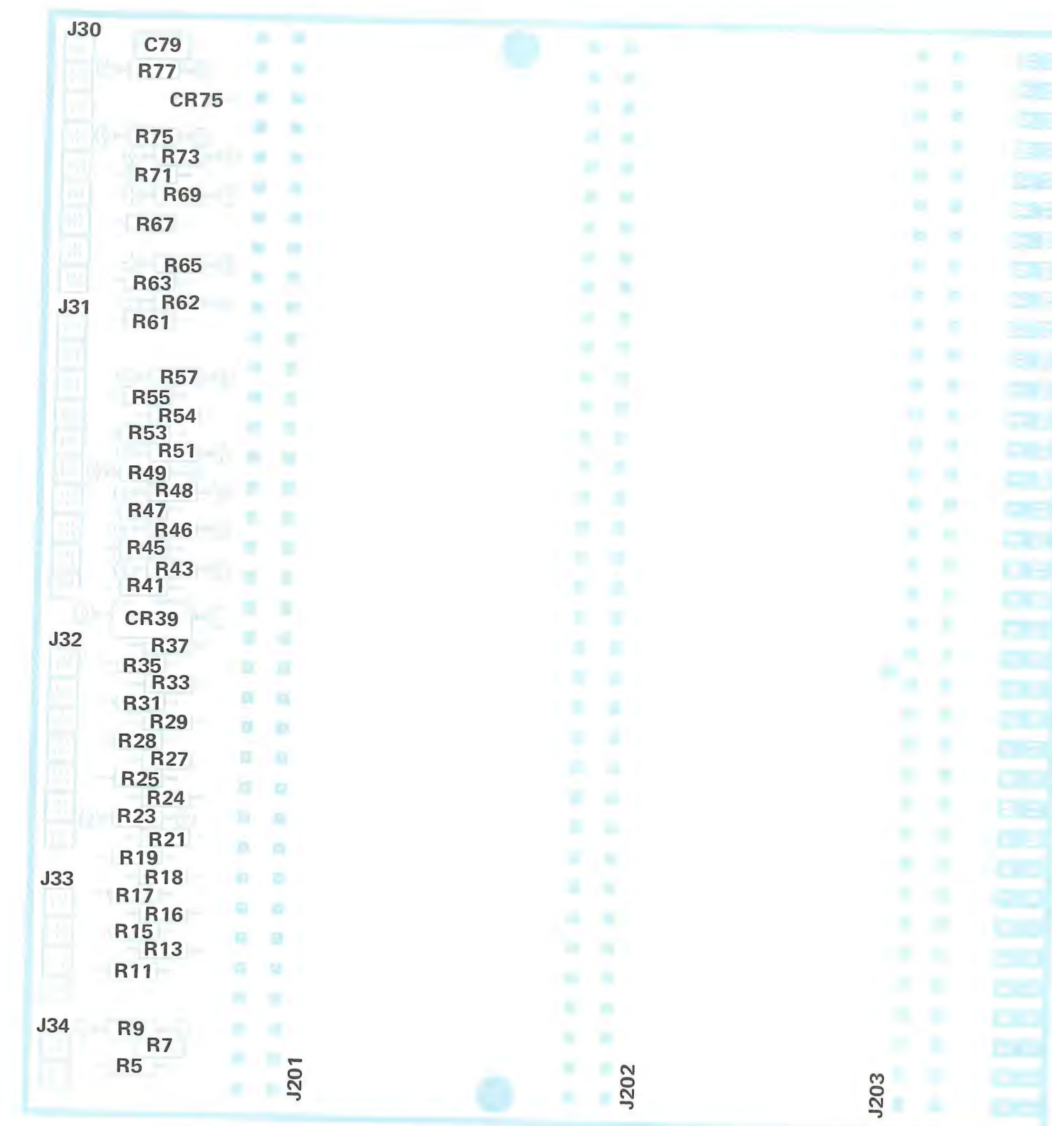


A3-MOTHER BOARD

FIG 6-3 MOTHER BOARD

4012

Ⓐ



Ⓐ

Fig. 6-4. Mother Board Component Location.

GENERAL INFORMATION

Introduction

The description of Terminal concepts and circuit operation is interleaved with block diagrams and circuit schematics. This type of layout is conducive to a quick understanding of the Terminal. It also doubles as a troubleshooting aid. All electrical data associated with any one circuit board is in one general area. This excludes the block diagrams that are used to provide acquaintance with the basics of Terminal/Computer communications and Terminal data flow.

This section also contains Semiconductor Information, a Wire List, and a Dictionary of Line Titles that will prove beneficial in understanding logic flow on the Interconnection Board (minibus). A Wire List Explanation shows how to use the Wire List in conjunction with the Connectors and Wiring Diagram and Interconnecting Board diagrams. The Dictionary of Line Titles should be read before any of the block diagram or circuit descriptions. The Wire List Explanation should be read before attempting to trace signals between schematics.

Diagrams and Circuit Description Information

The interleaving of the circuit descriptions with the block diagrams and schematics will allow those not familiar with Terminal operation to progress from a basic understanding to a fairly detailed understanding of Terminal concepts and operation. It is recommended that block diagrams and their respective descriptions be read in the following order.

1. Terminal/Computer Communication Concepts. This block diagram and description will provide acquaintance with the basics of Terminal/Computer operation. It will also introduce the basic electrical sections of the Terminal; namely the Keyboard, the Terminal Control section and the Display Unit.

2. Data Flow Block Diagram and Description. This block diagram explains the basic data flow within the Terminal. It shows the tie-in of the major electrical components for the Alphanumeric Mode, the Graphic Plot Mode, and the Graphic Input Mode.

3. Alphanumeric Mode Block Diagram and Description. This shows the operation and logic tie-in of TC-1 and TC-2 in the Alpha Mode.

4. Graphic Modes Block Diagram and Description. This provides the logic tie-in of TC-1 and TC-2 for Graphic Plot and Graphic Input (GIN) Mode operation.

5. Display Unit Block Diagram and Description. This block diagram and description gives a basic understanding of the circuitry associated with the Display Unit.

The above block diagrams and associated descriptions will, in most cases, aid in isolating a problem to a specific circuit card. In addition, they provide an indication of which individual circuits may be at fault.

The Display Unit circuit descriptions are interleaved with block diagram descriptions and detailed circuit descriptions. Detailed block diagrams and descriptions are given for both TC-1 and TC-2. Turn to the TC-1 Block Diagram, pull it out and notice that the entire block diagram is located to the left of the block diagram description. Now, pull the TC-1 schematic out to the right and unfold it. Notice that the blocks given on the block diagram correspond to the blocks indicated on the schematic. The specific components can be located by referring to the component location on the apron of the schematic. This layout of block diagram, schematic, and description provides all the information needed to locate and identify a specific component. The part number of the specific component can be found by referring to the Electrical Parts List in Section 5. TC-2 power supplies and the Display Unit circuits follow the same general outline.

DICTIONARY OF LINE TITLES

The following is a description of interconnecting (minibus) signals. A signal's active state is indicated by the signal name; i.e.: those with overlines indicate that the source must pull the signal line low to cause that function to occur.

Minibus Signal Line Definitions

$\overline{\text{AUXSENSE}}$. Status bit line reserved for auxiliary device(s). Disables graphic lookahead. The $\overline{\text{HCU}}$ bus line may also be used by auxiliary device(s) if no Hard Copy Unit is connected and powered up. Open collector source.

$\overline{\text{BIT 1}}$—$\overline{\text{BIT 8}}$. Data to and from the Terminal/CPU. See Fig. D-2 for timing. Open collector source; 48 mA load at 0.4 V.

$\overline{\text{BREAK}}$. Signal from the keyboard to the interface for computer signaling. Open collector source.

$\overline{\text{BTSUP}}$. Suppresses Terminal response to $\overline{\text{TSTROBE}}$. Should be asserted in response to $\overline{\text{CPUNT}}$ by devices (such as buffers used in error correction schemes) intended to intercept data on behalf of the Terminal. In such cases the assertion of $\overline{\text{BTSUP}}$ should be delayed 2 clock periods if it is desired to avoid interference with copy of locally generated data. Open collector source.

BXL. Buffered output of X Digital-to-Analog circuits. Does not include effect of vector filters.

BYL. Buffered output of Y Digital-to-Analog circuits. Does not include effect of vector filters.

$\overline{\text{CBUSY}}$. Indicates that the CPU (interface) is busy accepting a character. Controls the timing of coordinate data transmitted to the CPU. A low on $\overline{\text{CBUSY}}$ will not inhibit the keyboard, allowing keyboard interrupts when $\overline{\text{CPUNT}}$ is not asserted. Interfaces that must lock out the keyboard should do so with $\overline{\text{KLOCK}}$. Open collector source; 48 mA load at 0.4 V.

$\overline{\text{CGZSUP}}$. Suppresses Z signal from TC-1. Caused by $\overline{\text{END COUNT}}$ into TC-1. Also generated by Fast Vector option.

$\overline{\text{CPUNT}}$. Means data is about to be asserted by CPU (interface). Must be asserted at least 3.2 μs before data is placed on $\overline{\text{BIT 1—8}}$ and must remain low until after the trailing edge of the strobe(s) associated with the transfer. Open collector source.

CR. CARRIAGE RETURN; high active signal.

$\overline{\text{CSTROBE}}$. Strobes data to the CPU. Pulse width is 0.5 μs or more, synchronized to the clock. Must not occur more than 2 μs after $\overline{\text{CPUNT}}$ goes low. $\overline{\text{TSTROBE}}$ may be asserted simultaneously (from the same source) to provide local copy to the Terminal. Should not occur less than 0.5 μs after $\overline{\text{CBUSY}}$ goes false (+3 V). Open collector source; 48 mA load at 0.4 V.

$\overline{\text{CSUP}}$. Inhibits the interface from accepting $\overline{\text{CSTROBE}}$. This signal is used by devices such as line buffers, which need to intercept data destined for the CPU. Open collector source.

$\overline{\text{CURSE}}$. ESC SUB control character sequence creates this signal, which causes the crosshair cursor to appear.

$\overline{\text{DOWN}}$. Counting pulse for Y register. Open collector source.

$\overline{\text{DRBUSY}}$. Asserted by the Hard Copy Unit to set up the display for hard copy readout. $\overline{\text{DRBUSY}}$ should be asserted before the trailing edge of $\overline{\text{MAKE COPY}}$ in order to hold the Terminal busy during the scan. Also asserted by the Display Unit for the duration of the erase cycle, during which information may not be written on the screen. Open collector source; 48 mA load at 0.4 V.

$\overline{\text{ECHO}}$. Directs input sources to assert $\overline{\text{TSTROBE}}$ as well as $\overline{\text{CSTROBE}}$ when sending data to the CPU to provide a local copy on the screen of data entered into the CPU. Open collector source.

$\overline{\text{END COUNT}}$. Disables register stepping circuits and suppresses $\overline{\text{Z}}$ signal from TC-1.

$\overline{\text{EOL}}$. Indicates that the X Register is counting past the right margin. Used by the AUTO CR/LF logic. Asserting $\overline{\text{EOL}}$ will cause a CR/LF to be generated when in Alpha Mode. A Display Multiplexer could use this to shorten the right margin for small displays. In such use, EOL should not be asserted after CR is activated, to prevent random counting of registers. Open collector source.

$\overline{\text{FPAUSE}}$. Indicates that the X register has folded over in the process of CR, FF, RESET, or normal counting (X Right). Used to generate the pause required for proper operation of the Auto Line Feed circuit when used with a clocked interface. Also used internally on TC-2 for Interactive Graphics.

$\overline{\text{FUZZ}}$. Active state causes a switch from the Character & Vector Focus circuit to the Cursor Focus circuit during Alpha cursor or crosshair cursor writing. Open collector source.

Ⓐ

$\overline{\text{GIN}}$. When originated in TC-2, $\overline{\text{GIN}}$ indicates that the crosshair cursor is on, or that coordinate information is being transmitted to the CPU. Disables the Alpha cursor, Top-of-Page, and right margin CR/LF circuits. Sets Echoplex Suppression. Asserted by TC-1 or options when entering graphics, in order to ensure that the Character Generator is off (reset). Open collector source.

GND. Circuit ground.

$\overline{\text{GRAF}}$. Originates in TC-1 to indicate that Graphic Mode is set. Open collector source; 48 mA load at 0.4 V.

$\overline{\text{HCU}}$. Indicates that the Hard Copy Unit is capable of accepting a $\overline{\text{MAKE COPY}}$ request. Open collector source.

$\overline{\text{HIX}}$. Loads the HIGH X graphic byte into the X Register. Open collector source.

$\overline{\text{HIY}}$. Loads the HIGH Y graphic byte into the Y Register. Open collector source.

$\overline{\text{HOME}}$. Erases the display and selects Alpha Mode and Home position. Originated by keyboard HOME key or by TC-1. Open collector source; 48 mA load at 0.4 V.

$\overline{\text{INDICATOR 1}}$, $\overline{\text{INDICATOR 2}}$. Turns on the light-emitting diode (LED) indicators in the keyboard area. Open collector source; 48 mA load.

$\overline{\text{INQUIRE}}$. ESC ENQ control character sequence.

$\overline{\text{KLOCK}}$. Inhibits keyboard. Open collector source.

LCE. High active arming signal caused by ESC control character.

$\overline{\text{LEFT}}$. Counting pulse for X Register. Open collector source.

$\overline{\text{LOCAL}}$. Directs input sources to assert $\overline{\text{TSTROBE}}$, providing a screen display in the absence of computer echo. The interface(s) may also use this line. Originates in keyboard switch. Open collector source.

$\overline{\text{LOXE}}$. Loads the LOW X graphic byte into the X Register and triggers vector drawing. Open collector source.

$\overline{\text{LOY}}$. Loads the LOW Y graphic byte into the Y Register. Open collector source.

$\overline{\text{MAKE COPY}}$. Copy request; 866 μs wide minimum. Caused by $\overline{\text{MAKE COPY}}$ switch or by EXT ETB sequence. Open collector source.

MARG. Indicates that the Terminal is at Margin 1. With a directly connected interface, this corresponds to page full. High active.

$\overline{\text{NOLI}}$. Suppresses Linear Interpolation vector drawing and timing circuitry on TC-1 and TC-2. Asserted by TC-1 unless in Graph Mode. Open collector source.

$\overline{\text{PAGE}}$. Created by ESC FF control character sequence or PAGE key. Causes the display to erase the screen. Open collector source.

$\overline{\text{RIGHT}}$. Counting pulse for X Register. Open collector source.

$\overline{\text{SEND 8}}$. Directs the interface to accept full 8-Bit binary data instead of providing its own data for the 8th bit. The keyboard provides a fixed 8th bit that is true in standard factory-wired Terminals, but may be rewired false.

SPD 1. Spare connection.

$\overline{\text{SPEAK}}$. Audio connection to the loudspeaker. Other terminal of speaker is at +5 volts. Bypassed by a 0.01 microfarad capacitor. Open collector source.

$\overline{\text{SRH}}$. Contact closure for SHIFT key. Resets Hold status.

$\overline{\text{SW 1}}$. Asserted by keyboard switch SW 1. Open collector source.

$\overline{\text{SW 2}}$. Asserted by keyboard switch SW 2. Open collector source.

$\overline{\text{TAPEFETCH}}$. A pulse typically provided by some small computer interfaces to cause a paper tape reader or analogous device to read one byte of data. Open collector source.

$\overline{\text{TBUSY}}$. Indicates that the Terminal is busy executing a function such as writing, ringing the bell, etc. $\overline{\text{TBUSY}}$ controls the timing of data transmitted to the Terminal. Upon receipt of a byte of data, the Terminal will assert $\overline{\text{TBUSY}}$ by the trailing edge of $\overline{\text{TSTROBE}}$ if that byte is to make the Terminal busy. No condition, with the exception of MARG, will assert $\overline{\text{TBUSY}}$ except momentarily. (MARG can be patched out of $\overline{\text{TBUSY}}$.) The Terminal will, however, accept data if $\overline{\text{TBUSY}}$ is high or low, although the results in the low case are not defined. $\overline{\text{TBUSY}}$ does not inhibit transmission of data from the keyboard to the CPU. Open collector source; 48 mA load at 0.4 V.

$\overline{\text{TOPEN}}$. Disables Top-of-Page circuit, allowing an increased number of lines. Not brought out to minibus except by straps. Open collector source.

$\overline{\text{TSTROBE}}$. Strobes data into the Terminal, for execution by the Terminal. It is a pulse of 0.5 μs or longer, synchronized to the 614 kHz clock. Should not occur less than 0.5 μs after $\overline{\text{TBUSY}}$ goes false (+3 V). Open collector source; 48 mA load at 0.4 V.

$\overline{\text{TSUP}}$. Suppresses Terminal response to $\overline{\text{TSTROBE}}$. $\overline{\text{TSUP}}$ should be used by devices that need to blank the Terminal to incoming data, such as a paper tape punch when punching binary data. Open collector source.

$\overline{\text{TTY MASTER}}$. Used only when a dual communication interface installation exists.

$\overline{\text{UP}}$. Counting pulse for Y Register. Open collector source.

VIEW. Controls the flood guns in the CRT. A high turns the guns on. As long as the Terminal is in GIN or HCU, and for about 90 seconds after the last information sent to the Terminal, TC-1 will allow a steady high on VIEW. Otherwise, TC-1 places the display in Hold status by placing a 1200 hertz signal with 12.5% duty factor on VIEW. An optional device may place the display in non-store by pulling VIEW low. Open collector source.

X. Analog signal from TC-2 to display. −5 to +5 volts covers the screen. Positive signal corresponds to left deflection. Zero volts represents the physical center of the screen.

XMAT. Analog signal representing the X location within the character matrix. Originates on TC-1.

Y. Analog signal from TC-2 to display. −5 to +5 volts covers the screen. Positive signal corresponds to down deflection. Zero volts represents the physical center of the screen.

YMAT. Analog signal representing the Y location within the character matrix. Originates on TC-1.

$\overline{\text{Z}}$. Z-Axis Information. Open collector source; 48 mA load at 0.4 V.

4.9 MHz. Clock signal.

614 kHz. Clock signal.

WIRING INFORMATION

The following interconnecting references are provided to facilitate signal tracing:

Wire List—Explains signal paths through cables.

Connectors and Wiring Diagrams (Fig. 6-2)—Depicts locations and identity of connectors.

Minibus Diagrams (Figs. 6-3 and 6-4)—Shows connector locations on minibus and lists interconnecting lines.

Display Interconnect Diagram (Fig. 6-5)—Shows chassis circuitry and Display Interconnection Board signal distribution.

From/To Addresses (contained on schematics)—List source or destination of subject signal. Does not list interconnecting points.

For most purposes, signal tracing consists of reading the address from the line on the schematic, and going to that location. Since all cards on the minibus are interchangeable, addresses for these are simply listed as TO or FROM A3-BUS, followed by the specific pin number. These lines are applicable to all cards which can be inserted into the minibus connectors (TC-1, TC-2, Interface, Optional Extender, Accessory Cards).

In the event of cable trouble, it may be necessary to trace signals from point to point through all connectors. Start with the connector and pin number. If it is a harmonica connector, go to that connector in the Wire List. If it is a board-edge connector, go to that connector on the Mother Board diagram. Opposite the connector and pin number is listed the interconnecting point or points.

EXAMPLE 1. Follow $\overline{\text{HIY}}$ from TC-1 to its destination. Since $\overline{\text{HIY}}$ is on an interchangeable board, its P202-J connector is common to pin J on all cards connected to the Mother Board. To determine if the signal goes elsewhere, look on the Mother Board diagram under minibus pin J. No other points are listed.

EXAMPLE 2. Follow $\overline{\text{MAKE COPY}}$, which is generated on TC-1. Again, it is a connection on the minibus and goes to pin $\overline{\text{C}}$ on all minibus connectors. Look on TC-2 and the interface card to determine if it is used there. Then check the Mother Board diagram. It shows that minibus pin $\overline{\text{C}}$ also connects to J33-1. Going to J33 in the Wire List shows that pin 1 connects to P46 pin 3 in A4. Refer to A4 on the Interconnecting Diagram. The Interconnecting Diagram discloses that P35 pin 3 connects through P44-5 to the Make Copy switch, which also is a source for the signal. The Interconnecting Diagram also shows the signal going to J51-3. Refer once again to the Wire List. Note that the Wire List shows J51-3 connecting to J525-11. J525 can be identified by referring to the Connectors and Wiring Diagram. There it is determined that J525 is the Hard Copy Connector on the back of the Display Unit.

EXAMPLE 3. On the Keyboard schematic (Fig. 6-11) locate KSTROBE on P80-6. Go to the Wire List and find that it connects to P21-2 on assembly A2, the TC-2 card. Referring to TC-2 confirms this.

TABLE 6-1

WIRE LIST FOR CRT
J1

CONNECTORS		SIGNAL	TO OR FROM		ORIGINATING	WIRE
JACK	PIN	NAME	PLUG OR JACK	PIN	ASSEMBLY	COLOR CODE
J1	1	W. G. FIL	SOLDERED TO ASSEMBLY 6		A6	9-1
	2	W. G. FIL			A6	9-2
	3	W. G. CATHODE			A6	9-3
	4	CONTROL			A6	9-4
	5	FOCUS			A6	9-5
	6	ANODE 1			A6	9-6
	7	ANODE 2			A6	9-7

TABLE 6-2

WIRE LIST FOR TC-2 (A2)
J20 AND J21

ASSEMBLY 2 CONNECTORS		SIGNAL	TO OR FROM		ORIGINATING	WIRE
JACK	PIN	NAME	PLUG OR JACK	PIN	ASSEMBLY	COLOR CODE
J20	1	GND	80	8	A8	0-9
	2	XPOT	43	6	A4	4-9
	3	YPOT	43	2	A4	9-2
	4	K BIT 5 (b5)	80	11	A8	9-18

Table 6-2 is continued on the next page.

TABLE 6-2 (cont)

ASSEMBLY 2 CONNECTORS JACK	PIN	SIGNAL NAME	TO OR FROM PLUG OR JACK	PIN	ORIGINATING ASSEMBLY	WIRE COLOR CODE
	5	K BIT 4 (b4)	80	12	A8	9-26
	6	K BIT 3 (b3)	80	13	A8	9-28
	7	K BIT 2 (b2)	80	14	A8	9-27
J21	1	K BIT 1 (b1)	80	15	A8	9-25
	2	K STROBE	80	6	A8	9-0 Coax
	3	K BIT 6 (b6)	80	10	A8	9-17
	4	+5 V (K BIT 8)	80	5	A8	9-16
	5	K BIT 7 (b7)	80	9	A8	9-23
	6	SPARE	80	4	A8	9-35

TABLE 6-3

WIRE LIST FOR MINIBUS (A3) J30, J31, J32, J33, and J34

ASSEMBLY 3 CONNECTORS JACK	PIN	SIGNAL NAME	TO OR FROM PLUG OR JACK	PIN	MINIBUS	ORIGINATING ASSEMBLY	WIRE COLOR CODE
J30	1	GND	47	1 & 2	A & 36		0-4
	2	Y INPUT	47	5	$\overline{\text{P}}$		0N (8N Coax)
	3	$\overline{\text{FUZZ}}$	47	7	35	A 1 (TC-1)	9-36
	4	COAX GND	47	4			Shield (8N Coax)
	5	X INPUT	47	3	$\overline{\text{M}}$		2-N 8-N Coax)
	6	$\overline{\text{PAGE}}$	80	1	$\overline{\text{E}}$	A 8 & A 1	9-5
	7	VIEW	49	4	22	A 1	9-4
	8	SPD1 (SPARE)	49	7	21		9-34
	9	$\overline{\text{DR BUSY}}$	49	5	L	A 4	9-7
J31	1	$\overline{\text{INDICATOR 2}}$	46	4	$\overline{\text{N}}$	Console	9-05
	2	$\overline{\text{BREAK}}$	80	3	$\overline{\text{L}}$	A 8	9-14
	3	$\overline{\text{HCU}}$	47	6	$\overline{\text{J}}$		9-13
	4	$\overline{\text{HOME}}$	80	2	$\overline{\text{F}}$	A 8 & A 1	9-15
	5	$\overline{\text{SHIFT}}$	80	7	30	A 8	9-6
	6	$\overline{\text{INDICATOR 1}}$	46	5	25	Console	9-04
	7	$\overline{\text{SWITCH 1}}$	46	7	Z	Console	9-02
	8	$\overline{\text{SWITCH 2}}$	46	6	X	Console	9-03
	9	$\overline{\text{SPEAK}}$	41	1	19	A 1	9-3
	10	$\overline{\text{LOCAL}}$	46	9	H	Console	9-01
J32	1	+5 V	72		S	A 7	2-0
	2	+5 V	72		S	A 7	2-0
	3	+15 V	70	3	15	A 7	2-1
	4	−15 V	70	2	14	A 7	7-0
	5	5 V SENSE	No Conn				
	6	GND	75		A & 36	A 7	0-N
	7	GND	75		A & 36	A 7	0-N
J33	1	$\overline{\text{MAKE COPY}}$	46	3	$\overline{\text{C}}$	A 1 and Console	9-06
	2	$\overline{\text{PAGE}}$	49	3	$\overline{\text{E}}$	A 1 and A 8	9-12
	3	$\overline{\text{Z}}$	49	1	4	A 1 and A 4	9-N (Coax)
	4	SHIELD	49	2	A & 36		9-N (Shield)
J34	1	FAST VECTOR	46	1	R		9-7
	2	NO CONNECTION					

TABLE 6-4

WIRE LIST FOR DISPLAY INTERCONNECT AND DEFLECTION AMP & STORAGE (A4) J40, J41, J42, J43, J44, J45, J46, J47, J48, J49, J50, J51, J52, J53, J54, J55, and J56

ASSEMBLY 4 CONNECTORS JACK	PIN	SIGNAL NAME	TO OR FROM PLUG OR JACK	PIN	ORIGINATING ASSEMBLY	WIRE COLOR CODE
J40	1	POWER ON	Power Indicator Lamp		A 7	9-14
	2	NO CONNECTION				
	3	INDICATOR 1	Indicator 1 Plug			9-15
	4	INDICATOR 2	Indicator 2 Plug			9-16
J41	1	SPEAK	31	9	A 1	9-3
	2	+5 V	To Speaker		A 7	2-0
	3	SPEAK	To Speaker		A 1	9-3
	4	+5 V				No Wire
J42	1	−15 V	Both Cursor Pots		A-7	7-0
	2	Y POT	From Y Pot Wiper		Console	9-2
	3	NO CONNECTION				No Wire
	4	GND	All Keyboard Switches			0-N
	5	NO CONNECTION	And Power Lamp			No Wire
	6	X POT	From X Pot Wiper		Console	4-9
	7	+15 V	Both Cursor Pots		A 7	2-1
J43	1	−15 V	73	3	A 7	7-0
	2	Y POT	20	3	Console	9-2
	3	NO CONNECTION				No Wire
	4	GND	75	2		0-9
	5	+5 V	80	5	A 7	2-0
	6	X POT	20	2	Console	4-9
	7	+15 V	70	2	A 7	2-1
J44	1	+15 V	F. V. Pot			2-1
	2	FAST VECTOR	F. V. Pot			9-7
	3	+5 V	F. V. Pot			2-0
	4	SWITCH 4	Front Panel Switch		Console	3-N
	5	SWITCH 5				
		(MAKE COPY)	Front Panel Switch		Console	9-06
	6	GND (SW 4 & SW 5)	Front Panel Switch		Console	0-N
J45	1	INDICATOR 2	To Indicator 2		Console	9-05
	2	INDICATOR 1	To Indicator 1		Console	9-04
	3	SWITCH 2	From Console Rocker SW		Console	9-03
	4	SWITCH 1	From Console Rocker SW		Console	9-02
	5	SWITCH 3	From Console Rocker SW		Console	9-24
	6	LOCAL	From Console Rocker SW		Console	9-01
J46	1	FAST VECTOR	34	1		9-7
	2	SWITCH 4	*35	1	Console	3-N
	3	MAKE COPY	33	1	Console	9-06
	4	INDICATOR 2	31	1		9-05
	5	INDICATOR 1	31	6		9-04
	6	SWITCH 2	31	8	Console	9-03
	7	SWITCH 1	31	7	Console	9-02
	8	SWITCH 3	*35	2	Console	9-24
	9	LOCAL	31	10	Console	9-01

*Spare connector to be connected to TC Cards or Interfaces at a later date.

TABLE 6-4 (cont)

ASSEMBLY 4 CONNECTORS JACK	PIN	SIGNAL NAME	TO OR FROM PLUG OR JACK	PIN	MINIBUS	ORIGINATING ASSEMBLY	WIRE COLOR CODE
J47	1	GND	75				0-4
	2	GND	75				1-N
	3	X INPUT	30	5			9-1 Coax
	4	OPEN					
	5	Y INPUT	30	2			9-2 Coax
	6	$\overline{\text{HCU}}$	31	3	$\overline{\text{J}}$	A 4	9-13
	7	$\overline{\text{FUZZ}}$	30	3	35	A 1	9-36
J48	1	$\overline{\text{FUZZ}}$	62	3	35	A 1	9-36
	2	$\overline{\text{Z}}$ OUT	65	2		A 1 & A 2	9-N Coax
	3	GND	65	1			9-N Shield
	4	DYNAMIC FOCUS	62	2		A 4	9-3 Coax
	5	$\overline{\text{HC INT}}$	66	1			9-48
	6	GND					No Wire
J49	1	$\overline{\text{Z}}$ IN	33	3	4		9-N Coax
	2	GND	33	4			9-N Shield
	3	$\overline{\text{PAGE 2}}$	33	2	$\overline{\text{E}}$		9-12
	4	VIEW	30	7	22		9-4
	5	$\overline{\text{DRBUSY}}$	30	9	L	A 4	9-7
	6	DEF AMP GND	75				6-N
	7	SPD1	30	8			9-34
J50	1	GND					9-3 Shield
	2	DYNAMIC FOCUS	159	1			9-3 Coax
	3	−15 V	159	4		A 7	7-0
	4	GND	159	3		A 7	0-N
	5	+5 V	159	5		A 7	2-0
	6	+15 V	159	2		A 7	2-1
	7	TARSIG	159	6		A 9	9-4 Coax
J51	1	$\overline{\text{HCU}}$	525	13	$\overline{\text{J}}$	Hard Copy Unit	9-3
	2	$\overline{\text{WAIT}}$	525	14		Hard Copy Unit	9-5
	3	$\overline{\text{MAKE COPY}}$	525	11	$\overline{\text{C}}$	Console Switch	9-4
	4	$\overline{\text{READ}}$	525	9		Hard Copy Unit	0-9
	5	$\overline{\text{TARSIG}}$	525	7		A 4	9-1 Coax
	6	$\overline{\text{INTERROGATE}}$	525	5		Hard Copy Unit	9-2 Coax
	7	SLOW RAMP	525	1		A 4	2-N
	8	SLOW RAMP GND	525	2		A 4	0-N
	9	FAST RAMP GND	525	4		A 4	0-N
	10	FAST RAMP	525	3		A 4	2-N
J52	1	X DEFL	CRT Coil			A 4	2-N
	2	Y DEFL	CRT Coil			A 4	4-N
	3	Y DEFL	CRT Coil			A 4	5-N
	4	X DEFL	CRT Coil			A 4	6-N
J53	1	+200 FIL	71	1		A 7	2-3
	2	−20 V	78	2		A 7	7-1
	3	−15 V	73	2		A 7	7-0
	4	GND	75			A 7	0-N
	5	+5 V	72			A 7	2-0
	6	+15 V	70			A 7	2-1
	7	+20 V	76			A 7	4-N
	8	+175 V	71	5		A 7	9-0
	9	+328 V	71	3		A 7	9-5

TABLE 6-4 (cont)

ASSEMBLY 4 CONNECTORS JACK	PIN	SIGNAL NAME	TO OR FROM PLUG OR JACK	PIN	ORIGINATING ASSEMBLY	WIRE COLOR CODE
J54	1	−15 V	61	2	A 7	7-0
	2	GND	61	1	A 7	0-N
	3	+5 V	61	3	A 7	2-0
	4	+15 V	61	4	A 7	2-1
	5	+20 V			A 7	No Wire
	6	+175 V	61	5	A 7	9-0
	7	+328 V	61	6	A 7	9-5
J55	1	+20 V LIMITED	119	1	A 7	9-1
	2	−20 V	119	2	A 7	9-2
	3	CE 1	119	3	A 4	9-3
	4	OP LEVEL (STB)	119	4	A 4	9-4
	5	CE 2	119	5	A 4	9-5
	6	F. G. ANODE	67	1	A 4	9-6
	7	F. G. ANODE	119	6	A 4	9-7
	8	F. G. ANODE	67	2	A 4	9-18
	9	F. G. CATHODE	67	7	A 4	9-18
J56	1	X DEFL	To CRT Defl Coil			2-N
	2	Y DEFL	To CRT Defl Coil			4-N
	3	Y DEFL	To CRT Defl Coil			5-N
	4	X DEFL	To CRT Defl Coil			6-N

TABLE 6-5

WIRE LIST FOR HIGH VOLTAGE & Z AXIS (A6)
J60, J61, J62, J65, J66, J67, AND J68

ASSEMBLY 6 CONNECTORS JACK	PIN	SIGNAL NAME	TO OR FROM PLUG OR JACK	PIN	MINIBUS	ORIGINATING ASSEMBLY	WIRE COLOR CODE
J60	1	GND	75			A 7	0-N 8N TW/PR
	2	+20 V	76			A 7	2-N Coax
J61	1	GND	75			A 7	0-N
	2	−15 V	73	1		A 7	7-0
	3	+5 V	72			A 7	2-0
	4	+15 V	70	2		A 7	2-1
	5	+175 V	71	3		A 7	9-0
	6	+328 V	71	6		A 7	9-5
J62	1	GND					9-3 Shield
	2	DYNAMIC FOCUS	48	4		A 4	9-3 Coax
	3	$\overline{\text{FUZZ}}$	48	1	35	A 1	9-36
J65	1	GND	48	3			9-N Shield
	2	$\overline{\text{Z}}$	48	2	4	A 1 & A 2	9-N Coax
J66	1	$\overline{\text{HC INT}}$	48	5		A 4	9-48
J67	1	F. G. ANODE	54	1		A 4	9-18
	2	F. G. ANODE	54	2		A 4	9-18
J68	1	HC INTENSITY	HC Intensity Pot			Console	9-1
	2	HC INTENSITY	HC Intensity Pot			Console	9-0

TABLE 6-6

WIRE LIST FOR LOW VOLTAGE PWR SUP (A7) J70, J71, J72, J73, J75, J76, and J78

ASSEMBLY 7 CONNECTORS JACK	PIN	SIGNAL NAME	TO OR FROM PLUG OR JACK	PIN	MINIBUS	ORIGINATING ASSEMBLY	WIRE COLOR CODE
J70	1	+15 V	50	C		A 7	2-1
	2	(All pins)	43	7		A 7	2-1
	3		32	3	15	A 7	2-1
J71	1	+20 V LIMITED	50	1		A 7	2-3
	3	+328 V	50	9		A 7	9-5
	5	+175 V	50	8		A 7	9-0
J72	1	+5 V	32	1	S	A 7	2-0
	2	(All pins)	32	2	S	A 7	2-0
	3		50	5		A 7	2-0
J73	2	−15 V	32 50	4 3	14	A 7	7-0
	3	−15 V	43	1	14	A 7	7-0
J75	1		32	6		A 7	0-N
	2		32	7		A 7	0-N
	3		43	4		A 7	0-9
	4	GND	47	1		A 7	0-4
	5	(On all pins)	47	2		A 7	1-N
	6		49	6		A 7	9-34
	7		50	4		A 7	0-N
	8		60	1		A 7	0-N
J76	1	+20 V	50	7		A 7	4-N
	2	(Both pins)	60	2		A 7	2-N
J78	2	−20 V	50	2		A 7	7-1

TABLE 6-7

WIRE LIST FOR KEYBOARD (A8) J80

ASSEMBLY 8 CONNECTORS JACK	PIN	SIGNAL NAME	TO OR FROM PLUG OR JACK	PIN	MINIBUS	ORIGINATING ASSEMBLY	WIRE COLOR CODE
J80	1	$\overline{\text{PAGE}}$	30	6	$\overline{E}$	A 8 & A 1	9-5
	2	$\overline{\text{HOME}}$	31	4	$\overline{F}$	A 8 & A 1	9-15
	3	$\overline{\text{BREAK}}$	31	2	$\overline{L}$	A 8	9-14
	4	Spare −15 V	73				7-0
	5	+5 V	21	4		A 7	
	6	K STROBE	21	2		A 8	9-0 Coax
	7	$\overline{\text{SHIFT}}$	31	5	30	A 8	9-6
	8	GND	20	1			0-9
	9	K BIT 7 (b7)	21	5		A 8	9-23
	10	K BIT 6 (b6)	21	3		A 8	9-17
	11	K BIT 5 (b5)	20	4		A 8	9-18
	12	K BIT 4 (b4)	20	5		A 8	9-26
	13	K BIT 3 (b3)	20	6		A 8	9-28
	14	K BIT 2 (b2)	20	7		A 8	9-27
	15	K BIT 1 (b1)	21	1		A 8	9-25

TABLE 6-8

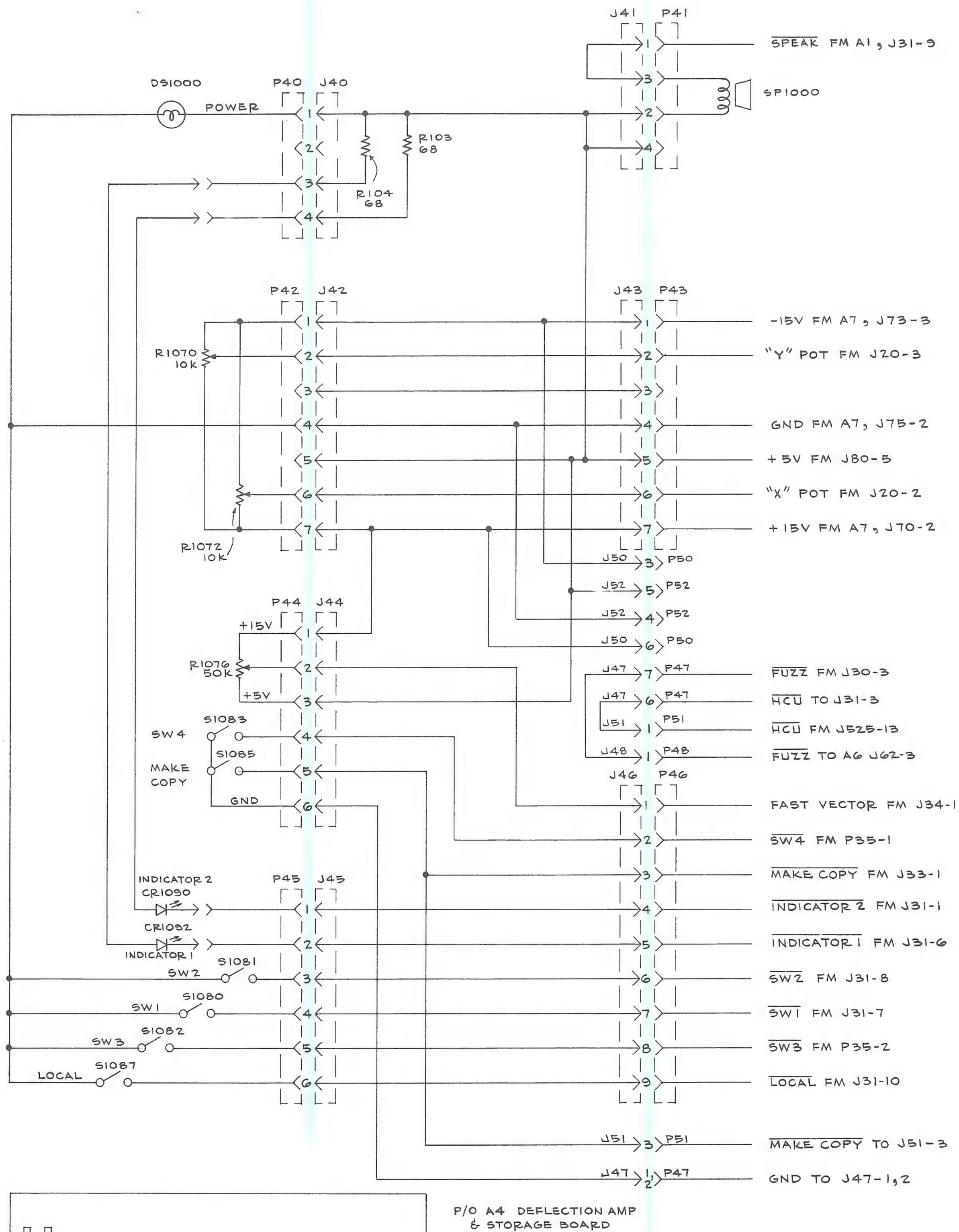
WIRE LIST FOR TARSIG HARD COPY AMPLIFIER (A9)
J119, J129, AND J159

ASSEMBLY 9 CONNECTORS JACK	PIN	SIGNAL NAME	TO OR FROM PLUG OR JACK	PIN	ORIGINATING ASSEMBLY	WIRE COLOR CODE
J119	1	+20 V Limited	J55	1	A 7	9-1
	2	−20 V	J55	2	A 7	9-2
	3	CE 1	J55	3		9-3
	4	OP Level (STB)	J55	4		9-4
	5	CE 2	J55	5		9-5
	6	F. G. ANODE	J55	6		9-6
	7	F. G. CATHODE	J55	7		9-7
J129	1	+20 V Limited	P2	1		9-1
	2	−20 V	P2	2		9-2
	3	CE 1	P2	3		9-3
	4	OP Level (STB)	P2	4		9-4
	5	CE 2	P2	5		9-5
	6	F. G. ANODE	P2	6		9-6
	7	F. G. CATHODE	P2	7		9-7
J159	1	DYNAMIC FOCUS	J50	2		9-3 Coax
	2	+15 V	J50	6	A 7	2-1
	3	GND	J50	4		0-N
	4	−15 V	J50	3	A 7	7-0
	5	+5 V	J50	5	A 7	2-0
	6	GND				9-4 Shield
	7	TARSIG	J50	7	A 4	9-4 Coax

TABLE 6-9

WIRE LIST FOR CHASSIS
J525

CHASSIS CONNECTORS JACK	PIN	SIGNAL NAME	TO OR FROM PLUG OR JACK	PIN	ORIGINATING ASSEMBLY	WIRE COLOR CODE
J525	1	SLOW RAMP	51	7	A 4	2-N
	2	SLOW RAMP GND	51	8	A 4	0-N
	3	FAST RAMP	51	10	A 4	2-N
	4	FAST RAMP GND	51	9	A 4	0-N
	5	$\overline{\text{INTERROGATE}}$	51	6	Hard Copy Unit	9-2 Coax
	6	OPEN				
	7	$\overline{\text{TARSIG}}$	51	5	A 4	9-1 Coax
	8	OPEN				
	9	$\overline{\text{READ}}$	51	4	Hard Copy Unit	0-9
	10	OPEN				
	11	$\overline{\text{MAKE COPY}}$	51	3	Console Switch	9-4
	12	OPEN				
	13	$\overline{\text{HCU}}$	51	1	Hard Copy Unit	9-3
	14	$\overline{\text{WAIT}}$	51	2	Hard Copy Unit	9-5
	15	CHASSIS GND			Terminal Chassis	To Solder Lug.



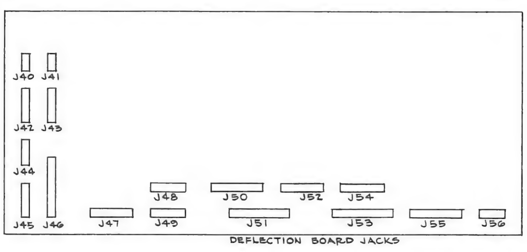


FIG 6-5, DISPLAY INTERCONNECTING DIAGRAM

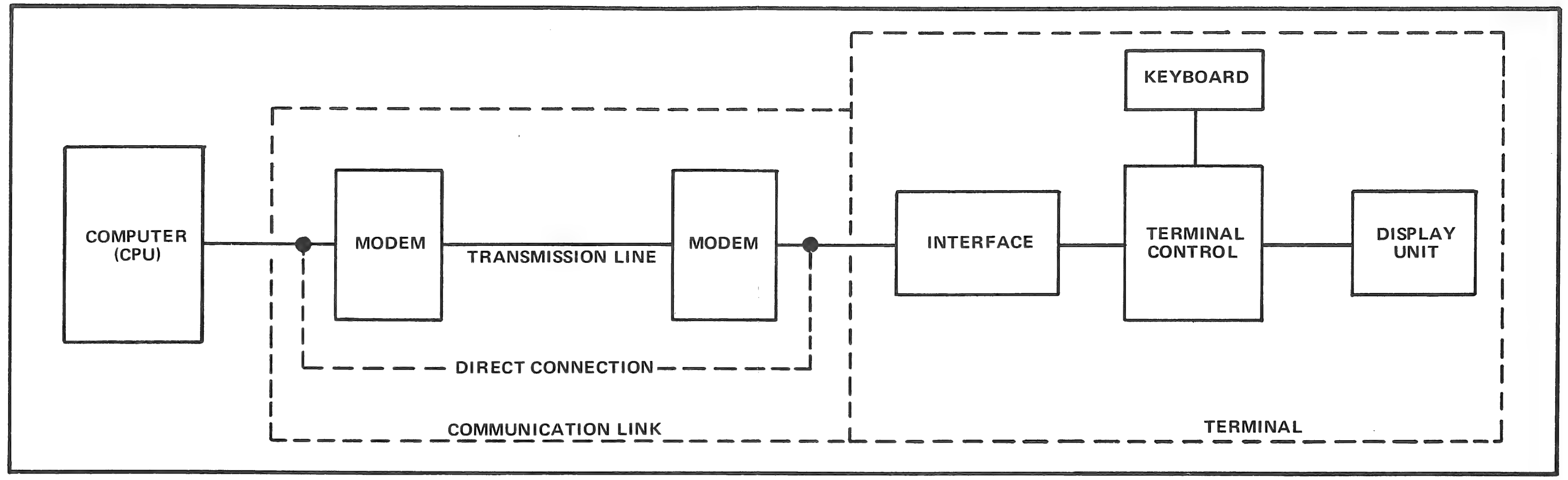


Fig. 6-6. Terminal/Computer Communications Block Diagram.

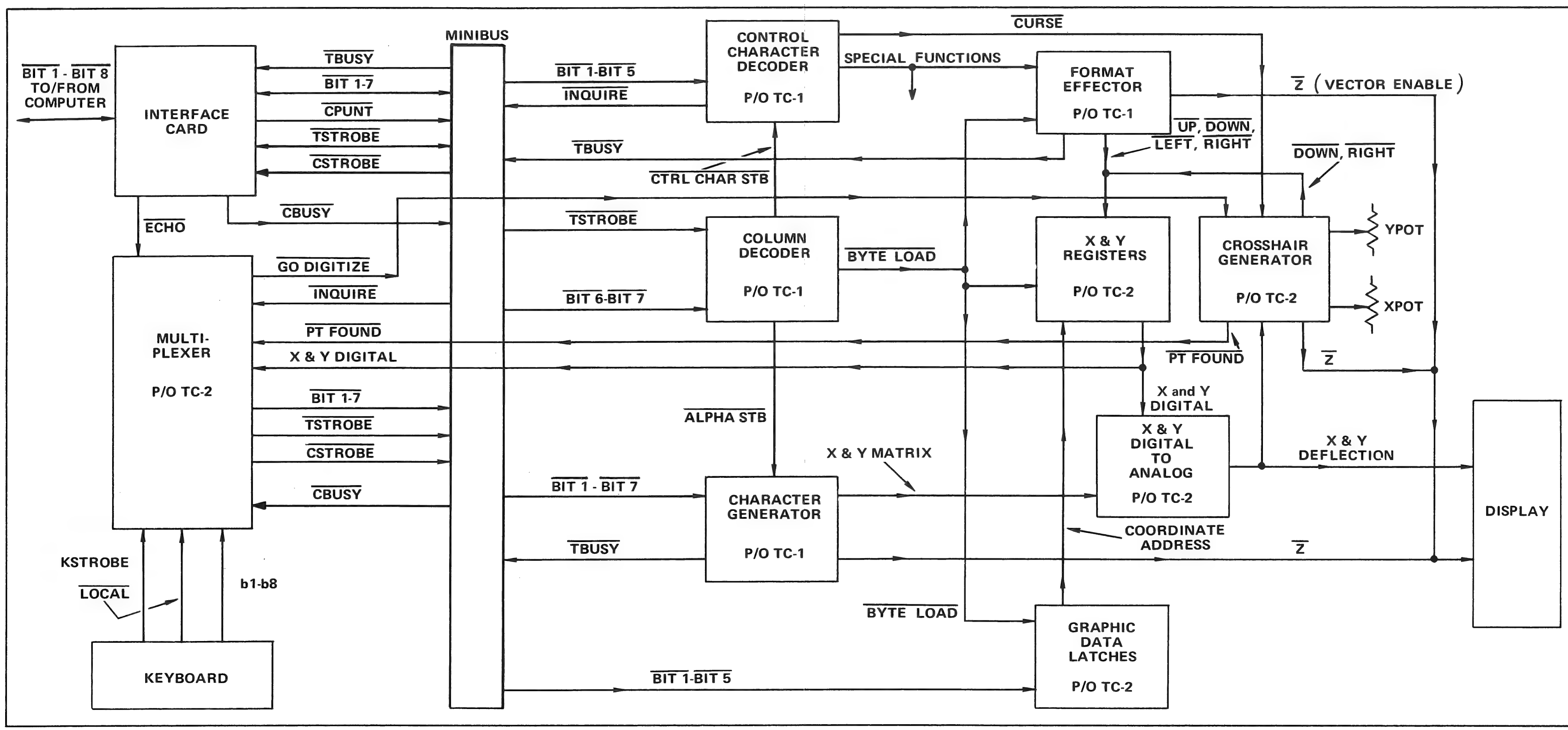


Fig. 6-7. Terminal Data Flow Block Diagram.

Ⓐ

BASIC CONCEPTS OF COMPUTER/TERMINAL COMMUNICATIONS

General

The Computer Display Terminal is a device that permits a person to deal directly with a computer. By using the keyboard (which is similar to a typewriter keyboard), a person can question or instruct the computer; the computer's response is returned to that person by way of the display screen, either alphanumerically or graphically (charts, graphs, pictures, etc.).

The Terminal/Computer Communications block diagram is shown in Fig. 6-6. The different sections are the Computer, the Terminal (which includes the Keyboard, the Display Unit, the Terminal Control circuitry, and the Communication Interface), and the Communication Link.

Computer

The computer can speak and act only through the use of binary numbers. The job of the computer then, is to accept data from the Terminal (commands from the Keyboard or other input devices), act on it by performing the indicated instructions, and return its response to the Terminal.

Terminal

The Terminal acts as a translator between the operator and a computer. Its job is to take the data from the computer and translate it into a language or graphic form that makes the data understandable to the operator.

Display Unit. The Display Unit presents data visually for both alphanumeric and graphic operation by accepting X and Y (writing beam position) and Z (writing beam on or off) signals from the Terminal Control circuitry. These signals combine in the Display Unit to give a visual representation on the display screen of the data interchange between the operator and the computer.

The Display Unit contains a storage-type CRT (cathode-ray tube). The data being displayed has only to be written once. The characteristics of the storage tube allow the image of the data to be retained for a long period of time (up to one hour without damage to the display screen) without having to continually redraw it, as would be necessary if a television-type CRT were used.

Keyboard. The Keyboard provides the operator with a readily understandable means of inputting data to the computer. It is an electromechanical device which, as a result of the operator's depressing any one of its keys, produces a binary data word that is distinctive for that key. This binary representation of the depressed key provides the Terminal Control and the computer circuits with a form of data they can understand.

Terminal Control. This circuitry accepts data from either the Interface or the Keyboard. This circuitry also provides synchronization so that the data is handled in the proper sequence. When data is accepted by the Terminal Control circuits, it routes this data to the computer and/or the Terminal Display Unit, depending upon the data source and the function requested by the data. The Terminal Control circuits interpret this data as either an alphabetic character or number, as coordinate points on an X-Y axis (for beam positioning), as a special function to be performed (backspace, ring bell, etc.) or as mode control information. Another function of the Terminal Control is to allow the Terminal status and the X and Y coordinates of any point on the display area of the screen to be sent from the Terminal to the computer when commanded to do so.

Interface

Direct. When the computer is located near the Terminal (as in the same building), a direct hook-up is the most practical.

Modem (Telephone Hook-up). In most cases the computer will be located a considerable distance from the Terminal, making a direct connection impractical. In such cases, the transfer of information between the computer and Terminal must be by other means. The most convenient and readily available means of transmission is the standard telephone line. However, the Terminal and computer cannot be hooked directly to the telephone because of the low frequency response of the telephone lines (computers can talk faster electrically than the highest frequency of the human voice); therefore, the telephone hook-up consists of a modulator-demodulator (MODEM) which places the data on a voice frequency tone (modulation) for transmission over the lines and retrieves the data (demodulation) at the receiving end. Both the computer end and the Terminal end of the telephone line have MODEMS. Both ends operate the same. Thus, by the use of telephone lines and the MODEM, the distant computer can be reached as easily as dialing a next-door neighbor.

DATA FLOW BLOCK DIAGRAM DESCRIPTION

General

Terminal logic operation is controlled by three logic cards. These are TC-1, TC-2, and Computer Interface. Each card has 72 interconnecting pins. Corresponding pins on each card are connected to one another by a plug-in connector board. This connector board is called a minibus. The minibus is designed to accommodate transmission between any devices connected to it.

Data is placed on eight data lines with open collector TTL buffers. The destination of data is determined by the use of strobe signals. Asserting a computer strobe ($\overline{\text{CSTROBE}}$) causes data to be transmitted to the computer via the Interface. Asserting a terminal strobe ($\overline{\text{TSTROBE}}$) causes data to be transmitted to the Terminal. Data may be sent to both by asserting $\overline{\text{CSTROBE}}$ and $\overline{\text{TSTROBE}}$ simultaneously. Strobe signals are normally synchronized with the system clock (614 kHz).

Timing of data is controlled by $\overline{\text{TBUSY}}$ (terminal busy), and $\overline{\text{CBUSY}}$ (computer busy). $\overline{\text{TBUSY}}$ and $\overline{\text{CBUSY}}$ control the rate of data transmission to devices responding to $\overline{\text{TSTROBE}}$ and $\overline{\text{CSTROBE}}$ respectively. The device receiving the data must enable its busy signal before the trailing edge of its respective input strobe, if it is to be considered busy. If the device transmitting the data does not sense a busy signal before the trailing edge, the transmitting device may presume that the data was accepted and could apply the next data immediately.

$\overline{\text{CPUNT}}$ (controlled by the Interface), controls the interleaving of data transmission. (Interleaving is the process of data being transmitted to and from the computer on the same data lines.) Data from the computer is preceded by $\overline{\text{CPUNT}}$ to inhibit the Terminal and any other device (other than the Interface card) from placing data on the minibus.

Transmitting Operation

Refer to the Data Flow Block Diagram in Fig. 6-7. When data is entered at the keyboard, the key pressed causes equivalent codes to be sent to the Multiplexer on seven parallel lines: b1—b7. An eighth bit accompanies them, and is always either high or low, depending on the way it is wired at the keyboard connector. A keyboard strobe signal termed KSTROBE accompanies the keyboard bits to the Multiplexer. KSTROBE causes the computer strobe signal ($\overline{\text{CSTROBE}}$) to go active, and causes the Multiplexer to place the keyboard bits on the minibus as $\overline{\text{BIT 1}}$—$\overline{\text{BIT 8}}$. Then $\overline{\text{CSTROBE}}$ strobes the bits into the Interface card, from where they are sent to the computer. If the $\overline{\text{ECHO}}$ signal from the Interface card is low, $\overline{\text{TSTROBE}}$ goes active along with $\overline{\text{CSTROBE}}$. This allows the Terminal circuitry to generate a "local" copy of the data sent to the computer.

Receiving Operation; Alpha Mode

When the computer sends data to the Terminal, a $\overline{\text{CPUNT}}$ signal appears to prepare the Terminal. Then $\overline{\text{BIT 1}}$—$\overline{\text{BIT 7}}$ are received, accompanied by $\overline{\text{TSTROBE}}$, which enters the Column Decoder. If a character is to be written, it is indicated by $\overline{\text{BIT 6}}$ and $\overline{\text{BIT 7}}$, which cause the circuit to generate an $\overline{\text{ALPHA STROBE}}$ signal. This signal latches character code bits $\overline{\text{BIT 1}}$—$\overline{\text{BIT 7}}$ into the Character Generator. The Character Generator sends X and Y MATRIX signals to the X and Y Digital-to-Analog circuits. $\overline{\text{TBUSY}}$ goes active at the same time, preventing reception of more data until the character is drawn. The X and Y DEFLECTION signals to the display change in accordance with the X and Y MATRIX signals. The decoded $\overline{\text{BIT 1}}$—$\overline{\text{BIT 7}}$ data bits cause Z signals to write at those matrix positions that are necessary for forming the character.

If the data bits contain the code for a Control Character, it is indicated by the $\overline{\text{BIT 6}}$—$\overline{\text{BIT 7}}$ combination, and detected by the Column Decoder. The Column Decoder then outputs a $\overline{\text{CTRL CHAR STB}}$ signal to the Control Character Decoder. This circuit decodes $\overline{\text{BIT 1}}$—$\overline{\text{BIT 5}}$ and inputs the indicated function signal. For example, if the data bits contain the code for a SPACE, the Control Character Decoder applies the SP signal to the Format Effector. The Format Effector outputs the required number of pulses on the $\overline{\text{RIGHT}}$ line. At the same time, $\overline{\text{TBUSY}}$ goes active until the function is completed, to prevent other activity. The $\overline{\text{RIGHT}}$ pulses increment the digital output of the X Register, causing the output of the X and Y Digital-to-Analog circuit to change accordingly. Thus, the display beam moves right one character space.

Refer back to the keyboard. A signal termed $\overline{\text{LOCAL}}$ inputs to the Multiplexer. If the Local/Line switch is in Local, $\overline{\text{LOCAL}}$ goes active and $\overline{\text{CSTROBE}}$ is inhibited. No data can be sent to the computer under this condition. Only $\overline{\text{TSTROBE}}$ will go active in response to keyboard inputs, and the results will be effectively the same as explained for Receiving Operation.

Receiving Operation; Graphic Plot Mode (Graph)

Graph Mode permits lines (vectors) to be drawn on the CRT by addressing the beam to a point on the display screen. As the beam moves to that point, the Z signal may go active to draw the vector.

Since the X and Y Registers each contain ten bits, twenty bits are required to address any position. These must be received in four bytes of five bits each, with each byte accompanied by two bits of steering data. The steering bits indicate X or Y, as well as whether the byte should be loaded as five most significant bits or five least significant bits. Data flow in the Graphic Plot Mode occurs in the following manner.

Refer to the Data Flow Block Diagram. When the Control Character bits for a GS (the signal that sets the Graph Mode) are received by the Interface card, TSTROBE and CPUNT go active. BIT 1—BIT 8 are then placed on the minibus. The Column Decoder is activated by TSTROBE and detects from BIT 6 and BIT 7 that a Control Character has been received. It then causes the CTRL CHAR STB signal to activate the Control Character Decoder, which then decodes the remaining data bits (BIT 1—BIT 5) and initiates the Special Function signals that set Terminal logic for Graph Mode. The next data bits received from the computer contain the first five bits of the coordinate address. BIT 6 and BIT 7 are decoded by the Column Decoder and the BYTE LOAD goes active, loading BIT 1—BIT 5 into the Graphic Data Latches. The next two bytes are received and loaded into the Latches in the same manner. With the reception of the fourth byte, all twenty bits of data (the Coordinate Address) are loaded into the X and Y Registers (10 into the X Register, and 10 into the Y Register). This causes the X and Y DIGITAL output of the X and Y Registers to change suddenly to the value set by the twenty bits of input data, causing the X and Y DEFLECTION output of the X and Y Digital-to-Analog circuits to change accordingly. At the same time the 20 bits of data are loaded into the X and Y Registers, the fourth BYTE LOAD pulse from the Column Decoder enables the Format Effector to output a Z (Vector Enable) signal. This turns on the display beam while the X and Y DEFLECTION signals change, causing a vector to be written. When the Z signal goes active, TBUSY also goes active to prevent the reception of more data from the computer until the vector is drawn.

Graphic Input Mode (GIN)

GIN Mode is used to send the Terminal status and/or graphic data to the computer. This may entail the generation of a full-screen crosshair cursor that can be positioned to any point on the viewable display area. The positioning of the crosshair cursor is performed by the use of two position controls (potentiometers) which are located to the right on the keyboard.

Refer to the Data Flow Block Diagram, Fig. 6-7. The control character sequence (ESC SUB) that initiates the GIN Mode is received from the computer and causes the Control Character Decoder to output a CURSE signal that is sent to the Crosshair Generator. The crosshair cursor is then drawn on the screen of the CRT in the following manner.

When initialized by the CURSE signal from the Control Character Decoder, the Crosshair Generator circuit sends DOWN pulses to the Y Register. These pulses cause the Y Register to decrement, moving the display beam downward. As the Y Register decrements with each pulse from the Crosshair Generator, the Y Digital output changes accordingly. The Y Digital-to-Analog circuit converts the Y Digital input to its comparative analog value, outputting it as the Y DEFLECTION voltage to the Display Unit. After each pulse, the Crosshair Generator sets the Z line active to draw the point. Notice that the X and Y DEFLECTION voltages are being sampled by the Crosshair Generator. When the deflection voltage just passes the voltage being input from Y POT (Y Position Potentiometer), the Crosshair Generator switches the count to the X axis. The Y Register then maintains its value while the X Register is being incremented by RIGHT signals from the Crosshair Generator. Like the Y Register, it increments until the X Deflection voltage just passes the voltage input from X POT (X Position Potentiometer). When this occurs, the circuit once again switches to the Y Register. The above-stated sequence repeats itself until the Terminal receives a command to send the intersection point to the computer.

The sending of the data to the computer can be done under user control, or computer control. When the user wishes to send the intersection point, he strikes a keyboard key. The keyboard character bits go to the computer as explained in the description of Transmitting operation. The Terminal will not be affected, because the Multiplexer does not generate a TSTROBE signal. CBUSY goes active during the time that it takes the computer to receive the data bits. When the computer completes the receiving process, CBUSY goes inactive. This causes the Multiplexer to send an active GO DIGITIZE signal to the Crosshair Generator. The next time the Crosshair Generator reaches the intersection point, it stops the counting sequence. The X and Y Registers are held at the digital equivalent of the X

and Y Position Potentiometer analog voltages. When the counting sequence stops, the Crosshair Generator sends a $\overline{\text{PT FOUND}}$ signal back to the Multiplexer. This causes the Multiplexer to send the 20 bits of X and Y Digital information to the minibus in four bytes. With each 5-bit byte, the Multiplexer sets $\overline{\text{BIT 6}}$–$\overline{\text{BIT 7}}$ low and generates the $\overline{\text{CSTROBE}}$ signal. This causes the data to be sent to the computer.

The computer can also request the coordinates of the crosshair cursor by sending the control character ESC followed by the control character ENQ (Inquire). When ENQ is decoded by the Control Character Decoder, the $\overline{\text{INQUIRE}}$ signal to the Multiplexer goes high. The operation of the Graphic Input circuitry is then the same as if $\overline{\text{CBUSY}}$ went inactive after a keyboard character had been sent.

If GIN Mode is used to send the Terminal status and the Alpha cursor or Graph Mode beam position, the crosshair cursor is not employed. Receipt of ESC ENQ while in either Alpha or Graph Mode results in the following action. The Control Character Decoder sends the $\overline{\text{INQUIRE}}$ signal to the Multiplexer, which places Terminal status bits on the $\overline{\text{BIT 1}}$–$\overline{\text{BIT 7}}$ lines, and generates a $\overline{\text{CSTROBE}}$ signal. The Interface Card generates $\overline{\text{CBUSY}}$ while it sends the status bits to the computer. When through, $\overline{\text{CBUSY}}$ ends. Its trailing edge causes the Multiplexer to remove the status bit from the $\overline{\text{BIT 1}}$–$\overline{\text{BIT 7}}$ lines. Again $\overline{\text{CSTROBE}}$ is generated and the Interface generates $\overline{\text{CBUSY}}$. When $\overline{\text{CBUSY}}$ ends, the second byte is sent and the operation repeats for the 3rd and 4th bytes. Since the Crosshair Generator was never turned on, the position register contents reflect either the Graph Mode beam position, or the Alpha cursor position, depending on the mode in which the Terminal is operating.

Regardless of what position information is sent (crosshair cursor, Alpha cursor, or Graph Mode beam), the Multiplexer may or may not send CR or EOT and CR, depending on option strap selection on TC-2. These are sent in the same fashion as the status bytes. When the transmission is complete, the Terminal returns to Alpha Mode if the crosshair cursor position or Alpha cursor position was sent. If the Graph Mode beam position was sent, the Terminal returns to Graph Mode.

ALPHA MODE
BLOCK DIAGRAM DESCRIPTION

General

When operating in Alpha Mode, the Terminal displays data in the form of alphanumeric characters. Some of the characteristics of character generation are:

1. The characters are generated by an 8 X 16 matrix contained within the Read Only Memory (ROM) device. The Character Generator uses 9 of the 16 available "row" outputs and 7 of the 8 available "column" outputs to write dots for character generation. The DEL character is suppressed with no spacing or printing.

2. Alphanumeric data can be displayed on 35 lines, with each line containing as many as 74 characters.

3. The Alpha cursor is a pulsating 7 X 9 dot matrix that indicates where the next character will be displayed.

4. There are two margins, termed Margin Ø and Margin 1. Margin Ø is located at the left side of the display screen and Margin 1 is located at the vertical center line of the display screen.

5. The Terminal performs an automatic Carriage Return and Line Feed when spacing past the end of a line.

The main purpose of the Alpha Mode Description is to show how the Terminal processes alphanumeric data for display purposes.

Power Initialization

Refer to Fig. 6-8, the Alpha Mode Block Diagram. When power is first applied, the Home circuit (located near upper center on the diagram) applies a low on the $\overline{\text{HOME}}$ line, placing the Terminal in Alpha Mode. Further switching to Alpha Mode occurs in the following manner.

When $\overline{\text{HOME}}$ goes low, it causes the Graf Flipflop to set $\overline{\text{NOLI}}$ active. With $\overline{\text{NOLI}}$ active, the X Filter and Y Filter are disabled, permitting the X Analog and Y Analog voltages to pass through to the Deflection Amplifier

circuitry unaffected. NOLI also enters the Column Decoder to allow the ALPHA STB signal to be generated.

Referring back to the HOME signal, notice that it also causes the output of U359C to go high. This sets the X Register to Ø and the Y Register to 767, causing the display beam to position to Home (upper-left corner of the display screen). A few milliseconds after initialization, when the power has stabilized, the HOME signal goes inactive.

The display screen "fades positive" at turn-on and must be erased before entering any data. This is accomplished by pressing the Page key. (For effect of PAGE on display circuits, refer to the Display Unit block diagrams and descriptions.)

Processing Control Characters

When the data bits of a Control Character are placed on the minibus, the TSTROBE signal is generated by the Multiplexer circuit (bottom-left corner). TSTROBE activates the TERM STB signal from the Terminal Strobe Gating circuit. The TERM STB signal enables the Column Decoder to process BIT 6 and BIT 7 (both are high when the data bits contain the code for a control character) and output an active control character strobe (CTRL CHAR STB) signal. This signal enables the Control Character Decoder. Data bits BIT 1—BIT 4, BIT 5, and the BIT 5 complement all input to the Control Character Decoder. The Control Character Decoder decodes the input data and activates the respective output line. For example, the Line Feed (LF) Control Character bits activate the LF signal.

The Escape circuit is shown as part of the Control Character Decoder circuit. This circuit makes it difficult to accidentally generate one of five signals — PAGE, CURSE, MAKE COPY, INQUIRE, and APL, which are the result of two character control sequences. First, the Escape (ESC) control character is received to prepare the Escape circuit for the next control character. This is followed by the control character that selects the specific function. For example, to activate the MAKE COPY signal (which activates the Hard Copy Unit) an ESC ETB sequence must be received. The decoding of ETB by the Control Character Decoder causes the enabled Escape circuit to activate the MAKE COPY signal. The remaining four output signals from the Escape circuit are similarly activated: ESC FF activates PAGE; ESC SUB activates CURSE; ESC ENQ activates INQUIRE; ESC SO causes APL; and ESC SI sets the APL line low. The Escape circuit is cleared when the clear signal from the Terminal Strobe Gating circuit goes active. This occurs every time the TSTROBE signal ends, unless the ESC character is being input. This means that the character following ESC disarms the circuit, regardless of whether or not it contains one of the commands of execution.

To backspace the Alpha cursor, the BS control character must be sent to cause the Control Character Decoder to activate the BS signal. BS then causes the Format Effector to output 14 pulses on the LEFT line. These pulses decrement the output of the X Register 14 counts, causing the output of the X Digital-to-Analog circuit to change its analog output value accordingly. This new value of X ANALOG voltage passes unaffected through the X Filter circuit (the Filter circuits are inhibited by NOLI) and causes the X Deflection Amplifiers to deflect the display beam one space to the left. Similar action occurs when the Terminal receives an HT control character. The only difference is that when HT is decoded, the HT signal goes active, causing the Format Effector to pulse the RIGHT line 14 times. The X Deflection Amplifier then deflects the display beam one space to the right.

To move the display beam up or down, the Vertical Tab (VT) or the Line Feed (LF) control characters must be sent. VT causes the Format Effector to pulse the UP line 22 times. LF causes the Format Effector to pulse the DOWN line 22 times. The resultant action from the Y Register through the Y Digital-to-Analog and Y Filter circuits is similar to that of the X circuits. The end result is to move the display beam either up or down one line.

TBUSY is activated when any of the input lines to the Format Effector go active. TBUSY is used by the Computer Interface Card to stop transmission from the computer to allow the Terminal to process the data and complete the intended operation. When the function is completed, TBUSY returns high.

Control characters such as BEL and CR cause the Format Effector to activate TBUSY for a predetermined period of time. BEL causes the Format Effector to output a 1200 Hz bell signal on the SPEAK line. When the predetermined span of time has elapsed, the Format Effector ends the SPEAK signal and at the same time ends TBUSY. The CR signal causes the Format Effector to output the CR signal and at the same time sets TBUSY active. CR inputs on the CLEAR input of the X Register, setting its outputs and the display beam to the predetermined margin position.

If $\overline{\text{GS}}$ has set the Graphic Plot Mode, the Alpha Mode can be re-established by sending any of the following Control Characters: US, CR, or ESC and FF ($\overline{\text{PAGE}}$). Pressing the Page or Reset keys will also re-establish the Alpha Mode. The above signals are input to the Graf FF to set $\overline{\text{NOLI}}$ active and $\overline{\text{GRAF}}$ inactive. The Format Effector activates $\overline{\text{TBUSY}}$ to give the Terminal logic time to reset to the Alpha Mode.

Processing Character Generation Data

The Character Generator circuitry is capable of generating 95 distinct ASCII alphanumeric characters. When no characters are being generated, the Character Generator outputs WRITE DOT, XMAT, and YMAT signals that draw the Alpha cursor. (The Alpha cursor indicates the beam writing position.) The operation of the Character Generator is as follows.

When $\overline{\text{TSTROBE}}$ goes active upon receipt of a character, the Terminal Strobe Gating circuit activates the $\overline{\text{TERM STB}}$ signal. $\overline{\text{TERM STB}}$ causes the Alpha Cursor Suppress circuit to set the SUPPRESS signal active. The SUPPRESS signal presets the YMAT and XMAT signals to put the display beam in the proper position to begin drawing the character.

The $\overline{\text{TERM STB}}$ signal also activates the Column Decoder which decodes $\overline{\text{BIT 6}}$ and $\overline{\text{BIT 7}}$ and outputs the Alpha Strobe ($\overline{\text{ALPHA STB}}$) signal. This allows the Character Generator to receive $\overline{\text{BIT 1}}$—$\overline{\text{BIT 7}}$, and at the same time sets the Character in Progress ($\overline{\text{CIP}}$) signal active. The $\overline{\text{CIP}}$ signal causes the Format Effector to set $\overline{\text{TBUSY}}$ active, thus preventing the reception of more data until the drawing of the character is completed.

Each of the characters that the Character Generator can produce has its own 8 X 9 dot matrix within a Read Only Memory (ROM) device in the Character Generator. Data bits $\overline{\text{BIT 1}}$—$\overline{\text{BIT 7}}$ are used to address the matrix of the specified character or symbol within the ROM. Timing signals from the Format Effector then cause the Character Generator to scan through the matrix one dot at a time. As the Character Generator scans the matrix, it outputs the XMAT and YMAT analog voltages which describe the point's location. These voltages are input to their respective Digital-to-Analog circuits to cause the Deflection Amplifier circuitry to position the display beam through the matrix.

As the ROM matrix is scanned, it indicates if a dot is to be written or not. The dot to be written causes the $\overline{\text{WRITE DOT}}$ signal to the Format Effector to go active. The Format Effector then outputs an active $\overline{\text{Z}}$ signal that causes the display beam to write a dot. The composite of the unblanked matrix dots forms the specified character on the display screen.

When the Character Generator has completed scanning the matrix, the Character Complete ($\overline{\text{CHAR COMP}}$) signal goes active. This causes the Format Effector to output 14 pulses on the $\overline{\text{RIGHT}}$ line, thus spacing the Alpha cursor to the next character position. The $\overline{\text{CIP}}$ signal ends, ending $\overline{\text{TBUSY}}$. The Terminal can now receive the next byte of data.

View Signal Operation

The purpose of the View Multi and Gating circuit and its associated VIEW signal is to prolong the life of the CRT. If no new data is being entered, after 90 seconds the VIEW signal is modulated by a 75 Hz, 12 1/2% duty cycle signal which reduces display intensity to put the Terminal in a Hold status. The Alpha cursor is suppressed during the Hold status. The View Multi and Gating circuit operates in the following manner.

The View Multi is basically a one-shot multivibrator that, when triggered, allows the VIEW signal to remain high for approximately 90 seconds. The View Multi is triggered each time the $\overline{\text{TERM STB}}$ signal causes the SUPPRESS signal to pulse high. If no data is entered within 90 seconds, the VIEW signal from the View Multi ends. This action places the 75 Hz signal on the VIEW line. A $\overline{\text{SHIFT}}$ signal entered at the keyboard can restore the VIEW signal.

Alpha Cursor Suppress

Four signals that suppress the Alpha cursor and hold VIEW high are:

$\overline{\text{DRBUSY}}$—Asserted by the Hard Copy Unit during character processing.

$\overline{\text{GRAF}}$—Asserted by the Graf Flipflop during graphic operation.

$\overline{\text{CIP}}$—Asserted by the Character Generator during duration of ALPHA STB.

$\overline{\text{GIN}}$—Asserted by the Multiplexer during GIN Mode.

During the active duration of the above signals, the XMAT and YMAT outputs hold the writing beam in the lower-left corner of the matrix.

Character Generator Inhibit

This circuit inhibits the Character Generator when $\overline{\text{GIN}}$ is active. ($\overline{\text{GIN}}$ remains active while GIN Mode is set.) This prevents the Character Generator from responding to the $\overline{\text{ALPHA STB}}$ signal caused by sending GIN Mode signals to the computer. For a more detailed explanation of the Graphic Input Mode, refer to the Graphic Operation Block Diagram Description. Refer also to the Description of the Echoplex Suppress circuit in the Block diagram description of TC-1.

The $\overline{\text{LOCAL}}$ signal from the keyboard goes active when the Local/Line switch is in the Local position. This sets the $\overline{\text{INH}}$ signal inactive, allowing the Character Generator to respond to alphanumeric data entered from the keyboard.

The $\overline{\text{TBUSY}}$ signal is also used to enable character generation. When the Graph Mode is activated, the GS signal momentarily pulls the $\overline{\text{GIN}}$ line low, causing the $\overline{\text{INH}}$ signal to go active. If it is desired to display alphanumeric data after switching out of Graph Mode, the Character Generator must be enabled. This is done by sending the CR or US control character to the Terminal, switching it to Alpha Mode. (Sending US allows the first alphanumeric character or symbol to be displayed at the ending point of the last vector. CR sets the beam to the left margin opposite the last vector ending point; the beam may also move down one line from that point if the CR EFFECT option is at CR→LF.) The same US or CR that ends the Graph Mode sets $\overline{\text{TBUSY}}$ active, causing the $\overline{\text{INH}}$ signal to go inactive, enabling the Character Generator to respond to $\overline{\text{ALPHA STB}}$ signals.

X Register

The X Register outputs 10 bits of BCD (Binary Coded Decimal) data, which provide a count from 0 to 1023. The register is capable of counting up or down to any number within this range. Each bit of data is input to the X Digital-to-Analog on its own line. (All ten lines are drawn as one on the block diagram.) In Alpha Mode operation, the signals that increment and decrement the X Register are $\overline{\text{RIGHT}}$ and $\overline{\text{LEFT}}$ respectively. Each pulse increments or decrements the count by one. The X Register is set to 0 when power is first applied ($\overline{\text{HOME}}$ goes active) or a $\overline{\text{PAGE}}$ or $\overline{\text{SHIFT}}$ signal is received. This causes the CLEAR signal from U359C to set all 10 output bits low, causing the display to position to the left hand margin. When the count increments to 1023, an End of Line ($\overline{\text{EOL}}$) signal is sent to the Format Effector. This causes the Format Effector to output a CR signal, clearing the register. Once again the display beam positions to the left hand margin.

Y Register and Top-of-Page Detect Operation

The operation of the Y Register is similar to that of the X Register. The main differences are as follows: When the Y Register is cleared, all its outputs go high; Pulsing the $\overline{\text{DOWN}}$ line decrements the count; Pulsing the $\overline{\text{UP}}$ line increments the count. Because the display screen is not as high as it is wide, not all the 1024 points are viewable, as they are for the X Register. Therefore, when the Y Register is cleared, the Alpha cursor is positioned off-screen beyond the top of the page. The purpose of the Top-of-Page Detect circuit is to decrement the count from the Y Register by pulsing the $\overline{\text{DOWN}}$ line until the Top-of-Page position is reached. The Top-of-Page position represents a Y Register count of 767, and is known as the Home position for the Y Register. It operates in the following manner.

When the Y Register outputs a count greater than 767 (1023 when it is cleared), the two Most Significant Bits of the Y Register (2 MSBY) are high. This activates the Top-of-Page Detect circuit which begins pulsing the $\overline{\text{DOWN}}$ line. When the count of 767 is reached, the 2nd MSB of the Y Register goes low, inhibiting the $\overline{\text{DOWN}}$ pulses. Thus, the Top-of-Page has been detected and the Alpha cursor is positioned in view at the top of the display screen.

Margin Shifter Operation

Left and Right margins are established by the lower and upper limits of the X Register. There is another margin that can be established at mid-page (X = 512) to provide for a two-column page. This effectively doubles the number of lines on which to enter data.

The Left Margin is referred to as Margin Ø and the center margin as Margin 1. Margin Ø is always established as a result of $\overline{\text{PAGE}}$ or $\overline{\text{HOME}}$ signals. The establishing of Margin 1 occurs in the following manner.

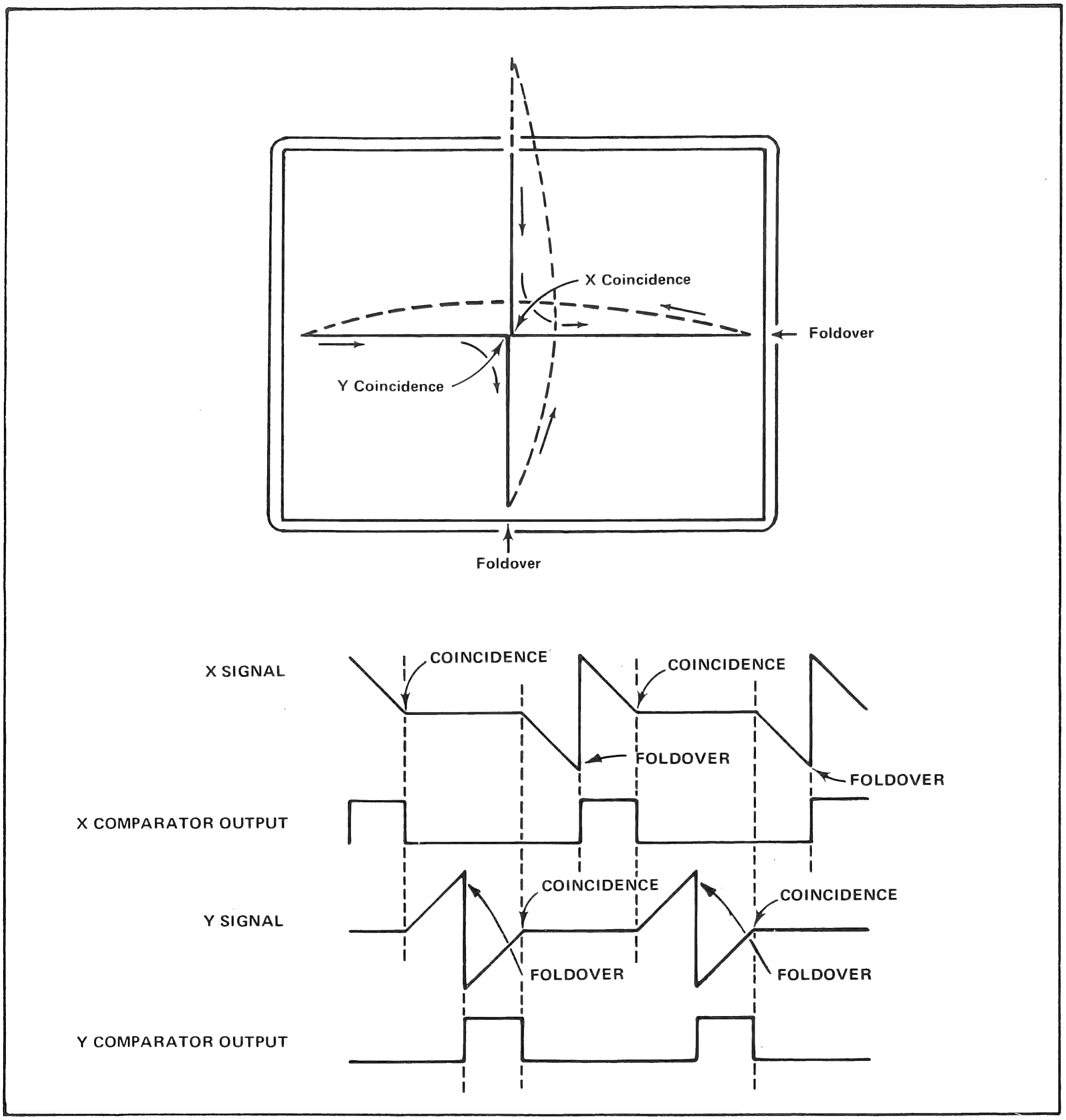
When the last line for Margin Ø has been reached and all desired data entered on that line, a CR and an LF code bit must be received by the Terminal to position the Alpha cursor to Margin 1. (The order in which they are sent is immaterial.) The LF causes the Y Register to space past the bottom line, which sets the MARG signal active. (The

MARG signal is actually an eleventh bit from the Y Register that carries a BCD weight of 1024.) When it goes active, it causes the MSB of the X Register (512) to remain high. This causes Margin 1 to be set. At the same time that LF causes MARG to go high, it causes the Top-of-Page circuit to activate. The combination places the Alpha cursor to the top center of the screen. (It should be noted that on all except the early TC-1 cards, strap options can be selected so that either LF or CR can cause both line feed and carriage return to occur.)

CR signals will not clear the Margin 1 position. This can be cleared by again spacing the Y Register past the bottom line of the page (unless PF BREAK is strapped IN). When this occurs, the MARG signal goes inactive. Margin 1 can also be cleared by activating the $\overline{\text{HOME}}$ or $\overline{\text{PAGE}}$ signals.

Digital-to-Analog Conversion

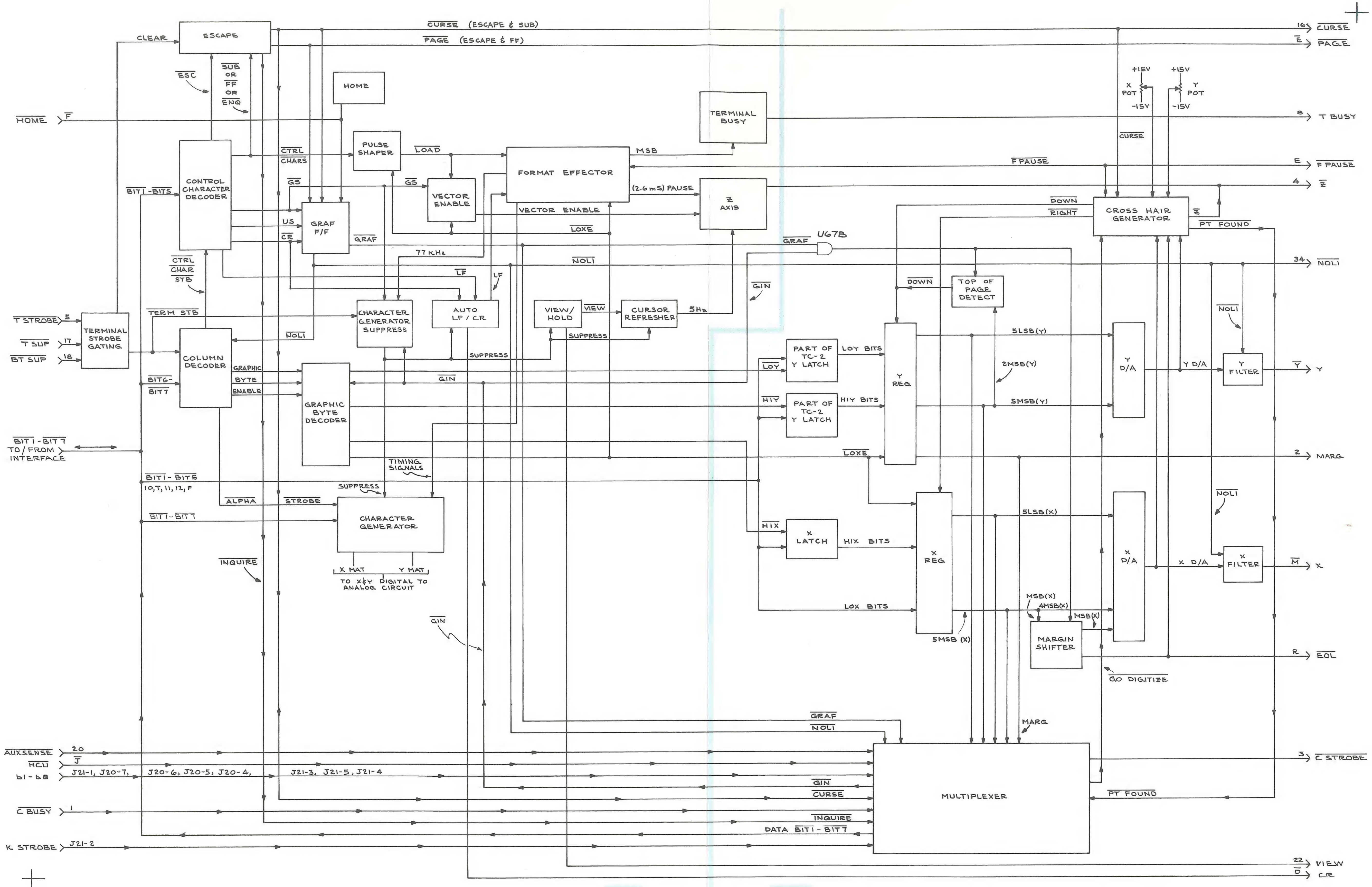
The X and Y Digital-to-Analog (D/A) converter circuits operate similar to each other. Their purpose is to convert the digital output of their respective registers into the equivalent analog voltage. These circuits also sum the XMAT and YMAT analog signals (from the Character Generator) with the X ANALOG and Y ANALOG signals, respectively. The outputs of these circuits pass directly through their respective Filter circuits (unaffected in Alpha Mode) and are input to the X and Y Deflection Amplifier circuitry to position the display beam.



Ⓐ

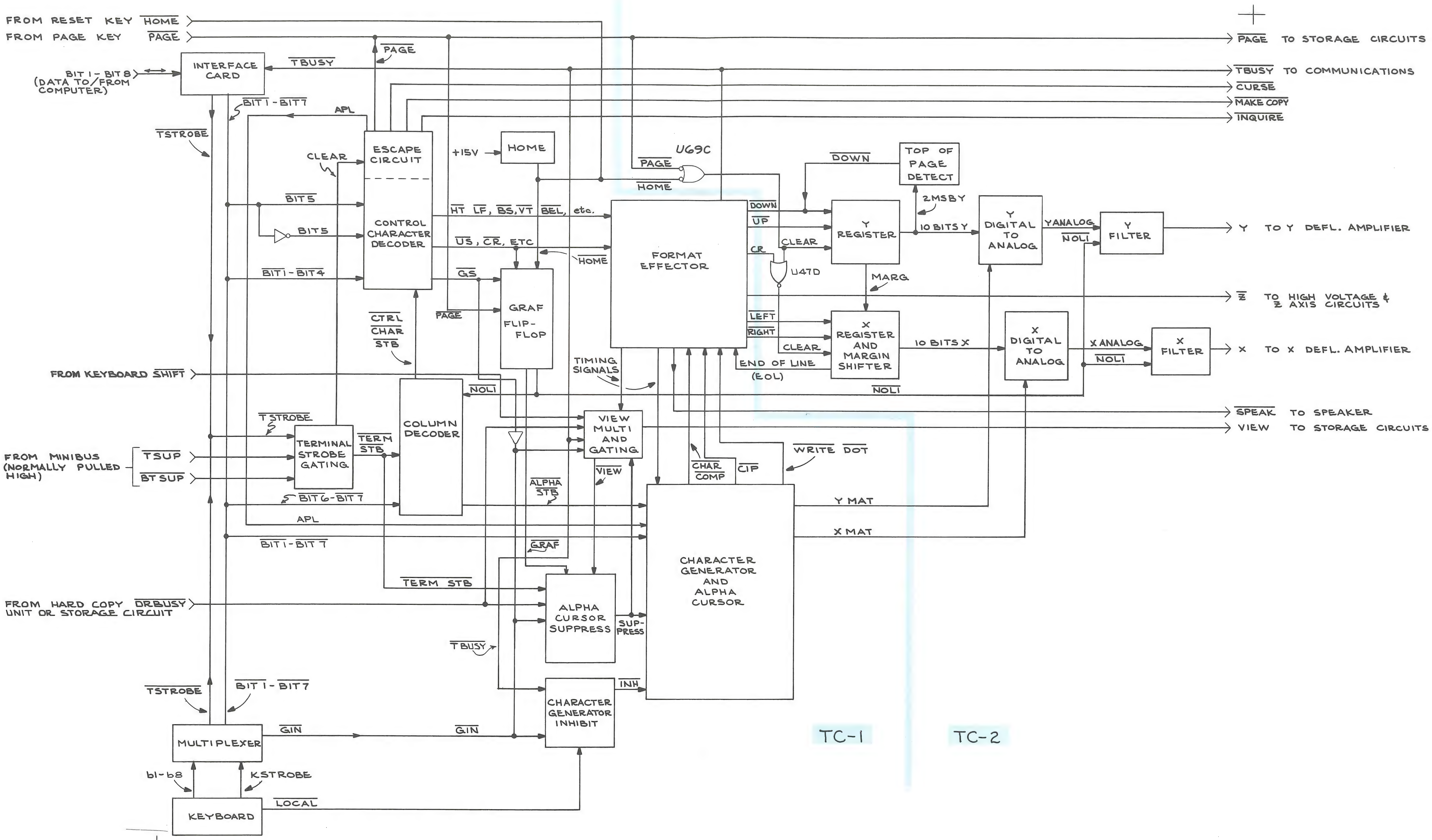
Fig. 6-10. Drawing a Crosshair Cursor Display.

GRAPHIC MODES
BLOCK DIAGRAM



TC-1 TC-2

FIG. 6-9 GRAPHIC MODES BLOCK DIAGRAM



4012

Ⓐ

FIG. 6-8 ALPHA MODE BLOCK DIAGRAM

ALPHA MODE BLOCK DIAGRAM

GRAPHIC MODES BLOCK DIAGRAM

General

The basic Terminal has two graphic modes. It can accept graphic data from the computer to draw vectors. This is termed Graphic Plot (Graph) Mode. It can send graphic data to the computer. This is known as Graphic Input (GIN) Mode.

Graphic data from the computer causes the Terminal to write vectors on the Display as specified by X and Y coordinate data. 20 bits of data are required to represent the axis address (10 bits for X and 10 bits for Y). The computer supplies this data to the Terminal as the five least significant bits of each of four 7-bit bytes. The two most significant bits are steering data.

Graph Mode Description

Refer to the Graph Mode Block Diagram in Fig. 6-9. Graph Mode operation is as follows.

Graph Mode Initialization. Terminal logic is designed so that when the Terminal is first turned on, the Home circuit sets all logic to the Alpha Mode. Notice the Home circuit of the Block Diagram (top-left corner). When power is first turned on (initialized), a $\overline{\text{HOME}}$ signal is generated. This causes the Graf Flipflop to output signals that set the Alpha Mode. $\overline{\text{GRAF}}$ goes high (inactive). $\overline{\text{NOLI}}$ goes low to inhibit the linear interpolation circuitry in TC-2. $\overline{\text{NOLI}}$ also inputs to the Column Decoder. Initialization of the Graph Mode begins with the control character GS. GS is usually entered under program control, but can be sent from the keyboard by pressing the CTRL and SHIFT and M keys simultaneously. For the purposes of this discussion, assume that the GS has been entered from the computer, and is placed on the minibus.

When the GS data is placed on the minibus, $\overline{\text{TSTROBE}}$ goes active to enable the Terminal Strobe Gating circuitry to input a low $\overline{\text{TERM STB}}$ signal to the Column Decoder. When $\overline{\text{TERM STB}}$ goes active, the $\overline{\text{CTRL CHAR STB}}$ signal is sent to the Control Character Decoder to allow it to process the GS contained on the $\overline{\text{BIT 1}}$–$\overline{\text{BIT 5}}$ lines at its inputs. The Control Character Decoder outputs a low $\overline{\text{GS}}$ signal to the GRAF Flipflop. This action switches the output states of the Flipflop; GRAF goes low, and $\overline{\text{NOLI}}$ goes high. $\overline{\text{NOLI}}$ going high enables the X Filter and Y Filter circuits.

Even though the $\overline{\text{NOLI}}$ input to the Column Decoder is high, the proper combinations of $\overline{\text{BIT 6}}$ and $\overline{\text{BIT 7}}$ will still generate the $\overline{\text{CTRL CHAR STB}}$. Thus, no matter whether operating in alpha or graphics, a $\overline{\text{CTRL CHAR STB}}$ can be generated to enable the Control Character Decoder.

Inhibiting the Alpha Circuits. In Graphic Plot Mode, the following Alpha Mode circuits are inhibited.

1. Character Generator
2. LF/CR
3. View/Hold
4. Cursor Refresher
5. Top-of-Page Detect
6. Margin Shifter
7. Margin 1

Explanations on how the above circuits are inhibited will be given in that order.

With $\overline{\text{NOLI}}$ set high, the Column Decoder is prevented from outputting an active $\overline{\text{ALPHA STB}}$ signal to the Character Generator. With the $\overline{\text{ALPHA STB}}$ inhibited, $\overline{\text{BIT 1}}$–$\overline{\text{BIT 7}}$ cannot be input to the Character Generator. $\overline{\text{GRAF}}$ also enters the Alpha Cursor Suppress circuit to cause a high-going SUPPRESS signal that resets the Character Generator to the Column 0, Row 1 position of the Character Matrix. Thus, the Character Generator is prevented from applying any voltages to the X and Y Digital-to-Analog circuits that might cause displacement of the beam while drawing a vector.

The same SUPPRESS signal that disables the Character Generator also disables LF/CR and View/Hold circuits. As long as the SUPPRESS signal is high, $\overline{\text{LF}}$ signals from the Control Character Decoder will not activate an automatic carriage return and line feed function. The high SUPPRESS signal inhibits the View/Hold circuit. This allows the displayed vectors to remain visible continually. (This is why the Terminal should be returned to Alpha Mode immediately after any plotting is finished to allow the View Multi to time the display into Hold.) The SUPPRESS signal is also input to the Cursor Refresher circuit to inhibit the generation of the Alpha cursor.

When $\overline{\text{GRAF}}$ goes low, the output of U345B inhibits the Top-of-Page Detect and Margin Shifter circuits.

Data Loading. $\overline{\text{BIT 1}}$—$\overline{\text{BIT 5}}$ are placed immediately at the input to the Y Data Latch with the arrival of the first coordinate data byte from the computer. $\overline{\text{BIT 6}}$ and $\overline{\text{BIT 7}}$ are decoded by the Column Decoder and Graphic Byte Decoder circuits. When the decoding occurs, $\overline{\text{HIY}}$ from the Graphic Byte Decoder goes low and strobes the five most significant bits of the Y coordinate address into the 5 MSB portion of the Y latch. As each following byte arrives on the minibus, $\overline{\text{BIT 6}}$ and $\overline{\text{BIT 7}}$ are decoded to enable the Graphic Byte Decoder to strobe the LOY and HIX bytes into their appropriate latches. With the arrival of the LOX byte, $\overline{\text{LOXE}}$ goes low. Notice that there is no latch for the LOX bits. The LOX bits are strobed directly into the X Register. With the arrival of the LOX byte, the $\overline{\text{LOXE}}$ signal simultaneously loads all twenty bits of coordinate data into the X and Y Registers. When $\overline{\text{LOXE}}$ ends, the output of the X D/A and Y D/A immediately change to the new coordinate position. Now that the outputs of the X D/A and Y D/A are at the new position, the display beam is turned on and the X and Y Filters begin linearly changing the X and Y signals to the new values.

Vector Enabling. $\overline{\text{LOXE}}$ also enters the Format Effector, Pulse Shaper, and Vector Enable blocks. In the Format Effector, $\overline{\text{LOXE}}$ is used as a preset input to time the 2.6 ms PAUSE signal that is used to activate the $\overline{\text{Z}}$ signal needed to draw the vector. The $\overline{\text{LOXE}}$ input to the Pulse Shaper generates the $\overline{\text{LOAD}}$ pulse that loads $\overline{\text{LOXE}}$ into the Format Effector. The first vector following a GS command is always dark because the VECTOR ENABLE output from the Vector Enable circuit is low, inhibiting the Z Axis circuit. With the arrival of the Low Order X bits of the next vector string, the VECTOR ENABLE signal goes high. This enables the Z Axis circuit to output an active $\overline{\text{Z}}$ signal to draw the vector. When the Format Effector has ended the 2.6 ms PAUSE signal, the $\overline{\text{Z}}$ signal is inhibited. Thus, the $\overline{\text{Z}}$ signal, combined with the movement of the X & Y inputs from the Filter circuits, causes the vector to be drawn.

A Z Control circuit is contained on TC-2 circuit cards numbered 670-1729-04 and above. This chops the Z signal during short vector drawing to reduce the vector intensity, making short vector intensity more consistent with long vector intensity. The $\overline{\text{LOXE}}$, $\overline{\text{NOLI}}$, X D/A, Y D/A, and three clock signals (not shown) are fed into the circuit to hold $\overline{\text{CGZ SUP}}$ high for vectors more than approximately one-half inch long, and to place a 12 1/2% duty cycle high on the $\overline{\text{CGZSUP}}$ line while vectors less than approximately one-half inch are being drawn.

Returning to Alpha Mode. When vector plotting is completed, it is best to return the Terminal to Alpha Mode. This allows the Terminal to time into Hold status to prevent possible damage to the Display Screen.

Alpha Mode is re-established by resetting the GRAF Flipflop. The following control characters will set Alpha Mode: CR, US, or ESC FF.

In addition, the following keyboard keys will reset the Terminal to Alpha Mode: Page or Reset.

GIN Mode Description

GIN Mode Initialization. Graphic Input Mode is set by the control character sequence ESC SUB. When they are received and decoded by the Control Character Decoder, the Escape circuitry outputs the $\overline{\text{CURSE}}$ signal. (See TC-1 discussion on Escape circuitry for description on operation of Escape.) $\overline{\text{CURSE}}$ inputs to the GRAF Flipflop to set $\overline{\text{NOLI}}$ low and $\overline{\text{GRAF}}$ high. $\overline{\text{NOLI}}$ going low inhibits the X & Y Filter circuits, thus allowing the outputs of the X & Y Filter circuits to pass directly through the Filter circuits unaffected. $\overline{\text{CURSE}}$ is processed in the Multiplexer circuitry, and causes the $\overline{\text{GIN}}$ output to go active. When $\overline{\text{GIN}}$ goes active it causes the SUPPRESS signal from the Character Generator Suppress circuit to go high. The LF/CR, View/Hold, and Cursor Refresher circuits are inhibited as previously explained in Graph Mode operation. $\overline{\text{GIN}}$ also inhibits the Graphic Byte Decoder during Graphic Input Mode. (The Column Decoder can still output the $\overline{\text{CTRL CHAR STB}}$ to the Control Character Decoder. Thus, control characters can still be processed.) The Top-of-Page Detect and the Margin Shifter circuits are also inhibited when $\overline{\text{GIN}}$ causes the output of U345B to go low. The Terminal logic circuitry is now set for GIN operation.

Crosshair Generator. When $\overline{\text{CURSE}}$ goes low, the Crosshair Generator becomes activated and begins sending $\overline{\text{DOWN}}$ pulses to the Y Register. Each time it pulses, it sends a short $\overline{\text{Z}}$ pulse to turn on the display beam. As the Y Register output decrements, it causes the output of the Y D/A to change accordingly. Thus, the display beam begins moving in the down direction. The output of the Y D/A is being sampled by the Crosshair Generator. When this voltage changes to the point where it just passes the voltage from the Y Position Potentiometer (Y POT), the counting pulses switch to the $\overline{\text{RIGHT}}$ line. This is known as "Y coincidence". The Y Register maintains its value while the X Register is incremented. The output of the X Register increments once with each low $\overline{\text{RIGHT}}$ pulse, causing the output of the X D/A to change accordingly. When the analog voltage input to the Crosshair Generator equals the voltage from the X POT, "X Coincidence" is reached. The count once again switches to the Y Register. Fig. 6-10 contains an illustration of crosshair cursor generation.

Foldover. If the X Register begins counting to the right of the X Coincidence Point, the count continues to increment the X Register until count 1023 is reached. When

this occurs, the Most Significant Bit (MSB) of the X Register causes the Margin Shifter to output an End of Line ($\overline{\text{EOL}}$) signal. This signal is input to the Crosshair Generator to inhibit the count of the X Register. This delay allows the display beam time to return to the left side of the display and stabilize before the count resumes. This is known as Foldover. The signal from the Crosshair Generator (as a result of this action) is $\overline{\text{FPAUSE}}$. It inputs to the Format Effector to inhibit its functions during the time $\overline{\text{FPAUSE}}$ is active (0.5 ms). The count then continues from 0 until X Coincidence is reached. When the count switches to the Y Register, the Crosshair Generator outputs $\overline{\text{DOWN}}$ pulses until the bottom of the page is reached. When this occurs, the beam folds over to the top of the page, but the Y Register continues to decrement with no Foldover Pause. No Foldover Pause is needed in the Y Axis, because Foldover positions the beam offscreen. By the time the beam appears in the display area of the screen, it has had time to stabilize. The Y Register continues decrementing until coincidence again occurs; the X Register starts incrementing and the cycle repeats itself until commanded to do otherwise.

Digitizing. When the user sends the Header Character, keyboard bits b1—b8 are inverted by the Multiplexer and placed onto the minibus lines as $\overline{\text{BIT 1}}$—$\overline{\text{BIT 7}}$. KSTROBE (which accompanied the keyboard bits) then generates the $\overline{\text{CSTROBE}}$ signal that strobes the data bits through the Interface card and to the computer. After the Header Character is accepted by the computer, the $\overline{\text{CBUSY}}$ line returns high, causing the $\overline{\text{GO DIGITIZE}}$ signal to go active. This causes the Crosshair Generator to stop the counting sequence when the next coincidence occurs. The digital representations of the voltages from the X and Y Position Pots are then held at the outputs of the X and Y Registers while the Crosshair Generator sends a $\overline{\text{PT FOUND}}$ signal back to the Multiplexer.

$\overline{\text{PT FOUND}}$ causes the Multiplexer to sample the 5 MSB X bits from the X Register and place them (along with code bits BIT 6 and BIT 7) on the minibus. Once again $\overline{\text{CSTROBE}}$ is generated and the byte is sent to the computer. When $\overline{\text{CBUSY}}$ again goes inactive, the 5 LSB X bits are sampled by the Multiplexer and the process repeats, sending the 5 MSB Y and then the 5 LSB Y bytes. These may be followed by CR or CR and EOT bytes if the circuit strap option is wired to do so. (EOT cannot be sent without CR.)

The computer can request the coordinates of the crosshair by sending an ESC SUB sequence (to initiate the GIN Mode as previously explained), followed by an ESC ENQ sequence. ENQ sets $\overline{\text{INQUIRE}}$ low, causing the Multiplexer to send the coordinates of the intersection point to the computer as previously explained. Note that the ESC SUB ESC ENQ sequence precludes transmission of the keyboard character.

The computer can also request the status of the Terminal by sending ESC plus ENQ while the Terminal is in Alpha or Graph Mode. In this case, only $\overline{\text{INQUIRE}}$ is activated and the Terminal status bits are sent in place of the keyboard character. They are followed by the location of the display beam (lower left corner of the Alpha cursor or Graph Mode beam address). The status bits appear on the $\overline{\text{BIT 8}}$—$\overline{\text{BIT 1}}$ lines as follows: 8 = Fixed by keyboard wire, 7 = Ø, 6 = 1, 5 = Hard Copy Unit status (on is Ø), 4 = Vector status (1 indicates set for vectors), 3 = Graph Mode status (Ø says Graph Mode exists), 2 = Margin (1 indicates Margin 1), 1 = Auxiliary sensing (Ø means an auxiliary device is activated).

KEYBOARD DESCRIPTION

General Description

Refer to the keyboard schematic. The keyboard consists of the following principal circuits: an oscillator, the 4 LSB Counter, the Character Detector, the 4 MSB Counter, the Character Decoder, the B5—B7 Control circuits, the Character Repetition Oscillator, and the Strobe Generator. Their combined purpose is to generate a coded character output on seven data lines labeled KB1 through KB7; to develop a strobe output labeled K STROBE (that accompanies the data bits); and to repeat the keyboard character at a 10 Hz rate when the key is held down more than 1/2 second.

Assume that characters are being entered at the keyboard. The oscillator generates a symmetrical output pulse which is applied to Z1 and Z10. Z1 causes the 4 LSB Counter to continuously cycle through its 16 counts. Each time it completes a cycle, it feeds a pulse to the 4 MSB Counter, causing it to advance one. The 4 MSB Counter eventually cycles through its 16 counts, and the entire performance is repeated. During this operation, the W output of the Character Decoder holds a low on the Z10 gate, causing the output of Z21 to remain high. This inhibits outputs from the Character Output Gates. KSTROBE is also held low during the operation.

When a character key is pressed, contact is made between an output of the Character Decoder and an input of the Character Detector. The output combination from

the 4 MSB Counter into the Character Decoder eventually reaches a code that selects the closed key. Since the 4 LSB Counter continues to cycle, a low is eventually placed on the closed key. This low is applied to the Character Detector, causing its W output to go high. This high provides enabling voltage to Z10 in the Strobe Generator. When the Ø1 output of the oscillator goes high, it causes a positive-going INHB pulse of about 22 ms from the strobe Generator. An INHA pulse from Z10 is input to the oscillator to prevent additional clock pulses from affecting the 4 LSB Counter.

With the count from the 4 LSB and 4 MSB Counters frozen, the B5, B6, and B7 logic circuits place the decoded equivalents of the $\overline{B5}$, $\overline{B6}$, and $\overline{B7}$ information on their respective output Gates. Approximately 22 ms later the INHB goes low, providing an enabling voltage for the Character Output Gates. This action places on the B1–kB7 lines the representative bit combination of the character pressed. $\overline{INHB}$ going low enables the KSTROBE signal that accompanies the data bits.

$\overline{INHB}$ also triggers the Character Repeat Oscillator. If the same key is held down for more than .5 second, the Character Repeat Oscillator strobes Z21 in the Strobe Generator at an approximately 10 Hz repetition rate. This enables KSTROBE 10 times a second . . . thus enabling the terminal to process the character bits at that rate.

The keyboard circuitry maintains the above-stated condition as long as the keyboard key is held down. When the key is released, the high from the W output of the Character Detector is removed from Z10, permitting its output to return to its high state. This ends the B1–B7 and KSTROBE outputs.

Miscellaneous Functions

SHIFT, CONTROL, and TTY keys. Pressing one of these keys causes the outputs of the B5–B7 Control circuits to reflect the appropriate bit configuration for the character code desired. For example, pressing SHIFT in conjunction with an alpha key causes the output configuration of B1–B7 to represent the upper-case alpha character. Pressing the CONTROL (CTRL) key causes the output bit configuration to represent a control character. And pressing TTY permits only upper-case alpha bit configurations to be structured.

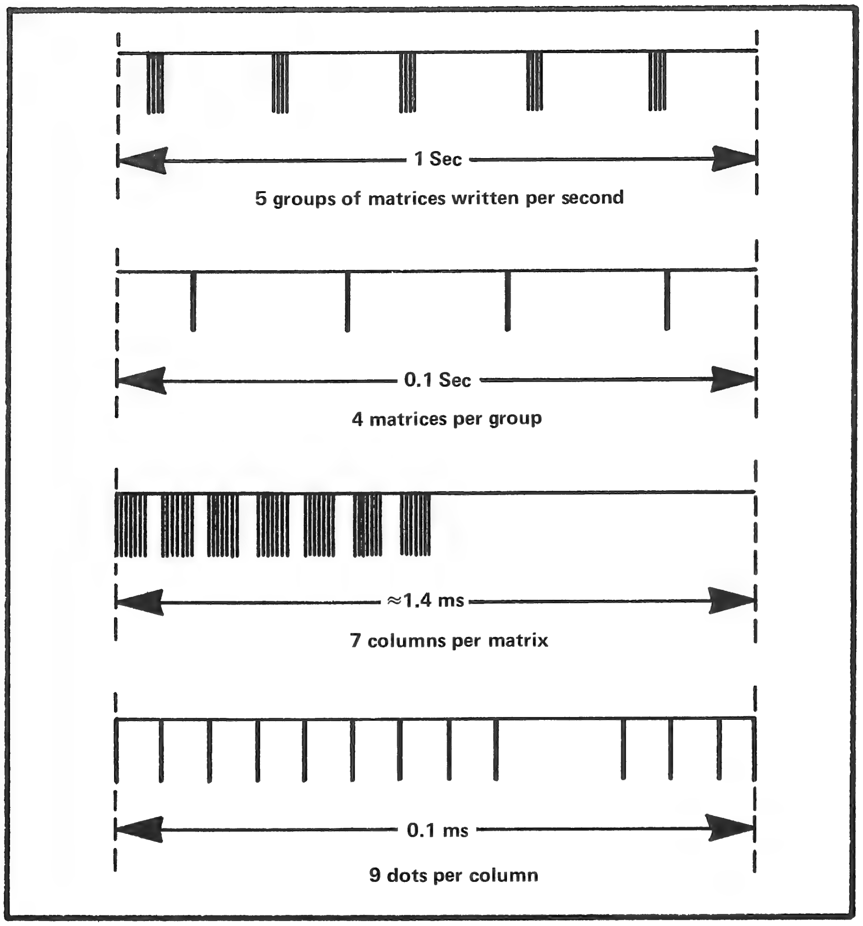


Fig. 6-13. Z Axis Signals During Alpha Cursor Refresh Time.

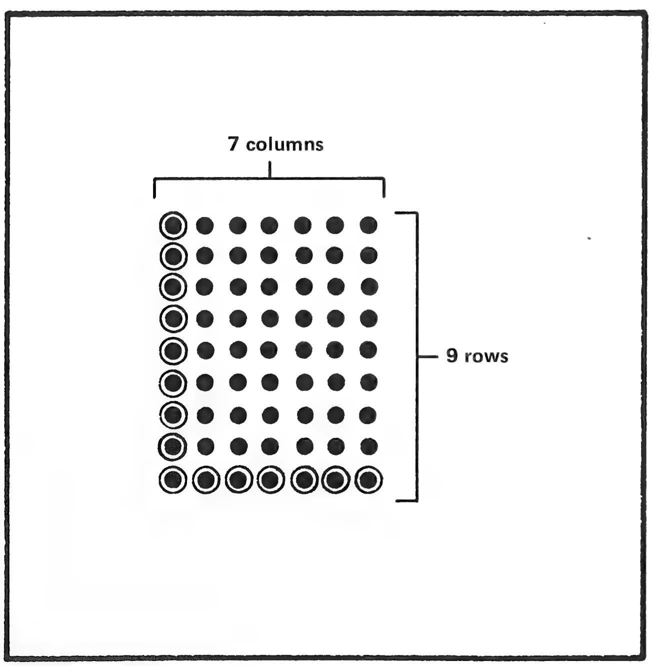


Fig. 6-14. Dots indicate matrix positions for character writing. Circles indicate which dots are written to form the letter L.

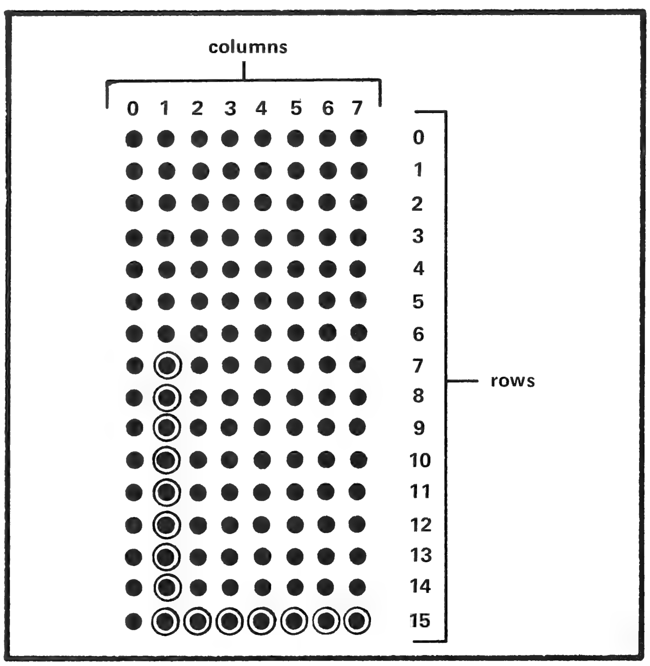
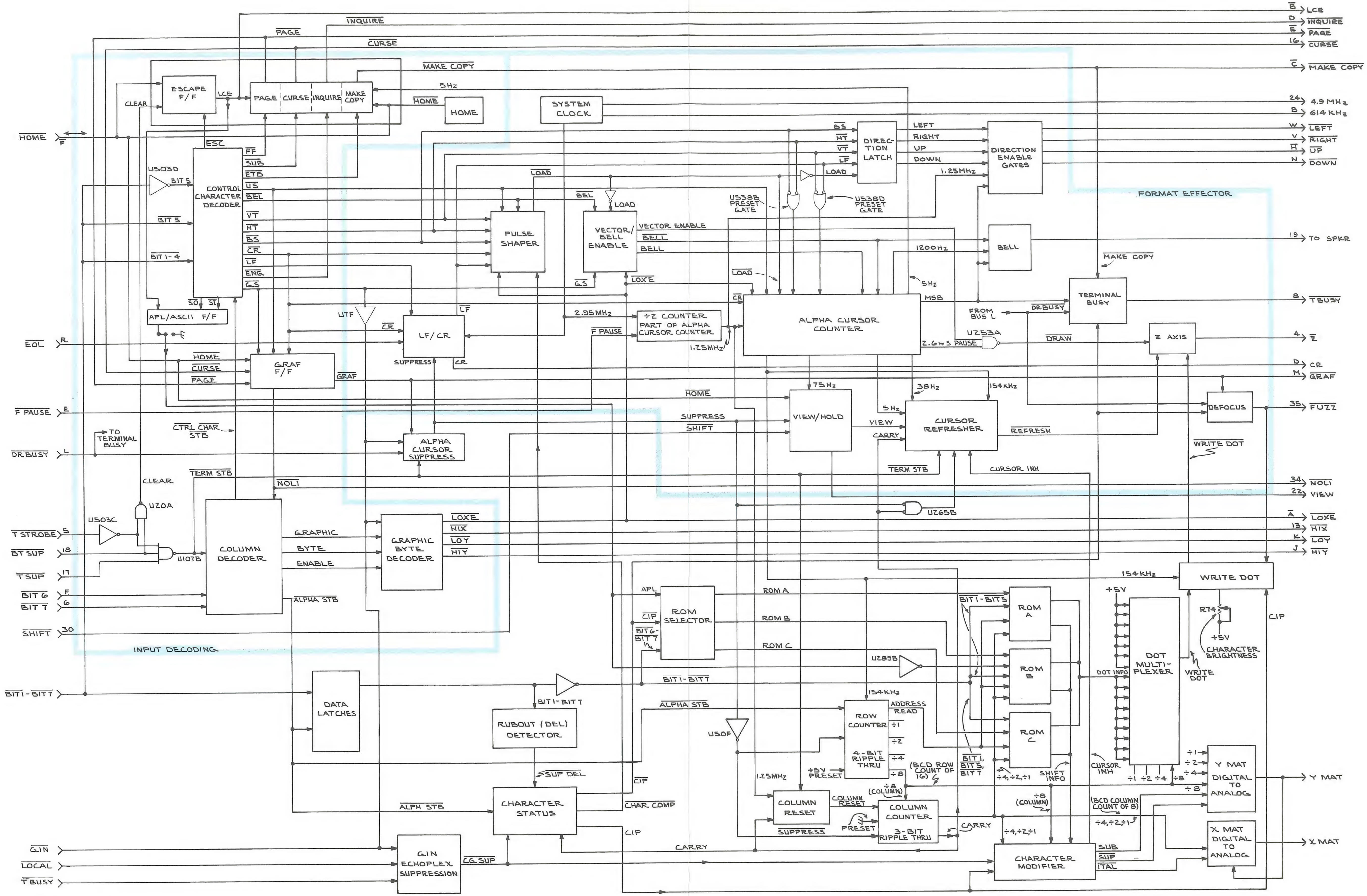


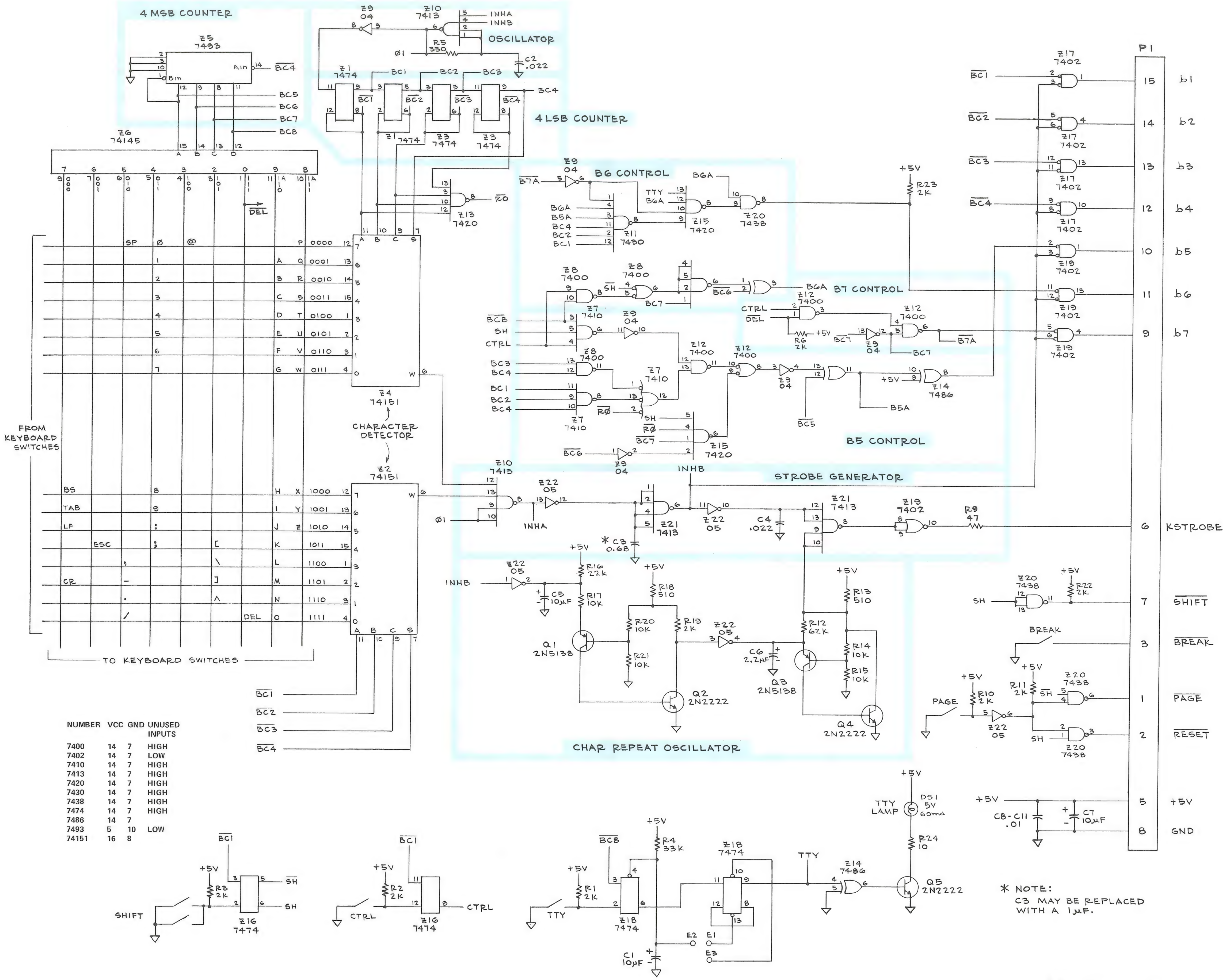
Fig. 6-15. Dots indicate the matrix generated by the Row Counter and Column Counter. No dots can be written when column 0 or row 0 through row 6 are selected.



4012

FIG. 6-12 TC-1 DETAILED BLOCK DIAGRAM

TC 1 BLOCK DIAGR



NUMBER	VCC	GND	UNUSED INPUTS
7400	14	7	HIGH
7402	14	7	LOW
7410	14	7	HIGH
7413	14	7	HIGH
7420	14	7	HIGH
7430	14	7	HIGH
7438	14	7	HIGH
7474	14	7	HIGH
7486	14	7	
7493	5	10	LOW
74151	16	8	

* NOTE:
C3 MAY BE REPLACED WITH A 1µF.

KEY TRONIC CORP.

FIG 6-11 KEYBOARD

TC-1 BLOCK DIAGRAM DESCRIPTION

Introduction

The operation of TC-1 can be best understood when it is broken down into three basic blocks of operation. These blocks are called Input/Decoding, Format Effector, and Character Generator. The three sections will be discussed in detail, in that order. Basically, the Input/Decoding section decodes the various input signals and data for Terminal operations. The Format Effector section is used to initiate a number of functions mainly associated with Alpha Mode. The Character Generator section generates the alphanumeric characters and symbols.

Input Decoding

General. Refer to TC-1 Block Diagram Fig. 6-12, and Schematic Fig. 6-17. The Input/Decoding section contains the following circuits:

Home—When power is turned on, this circuit outputs the HOME signal that sets Terminal logic to Alpha Mode.

Column Decoder—Generates signals that enable the Control Character Decoder, Character Generator, or Graphic Byte Decoder circuits.

Control Character Decoder—Decodes control characters used by the Terminal.

Escape Flip-Flop—Prevents accidental activation of $\overline{\text{PAGE}}$, $\overline{\text{CURSE}}$, $\overline{\text{MAKE COPY}}$, and $\overline{\text{INQUIRE}}$ signals. Also used ,in character selection if option strap is in AB+BC position.

Page, Curse, Make Copy, and Inquire Circuits—Used in conjunction with Escape Flip-flop to prevent accidental activation of their respective outputs.

Graf Flip-Flop—Sets Graphic Plot Mode.

Graphic Byte Decoder—Activated during Graphic Plot Mode to strobe coordinate address bytes into proper latch on TC-2.

The description of the Input/Decoding section will be given in that order. For the purpose of the description, assume that data is present on the minibus.

Home. Refer to the upper left corner of the block diagram. The purpose of this circuit is to reset all logic to the Alpha Mode when power is turned on (initialized). When power is turned on, the Home circuit applies a low pulse on the $\overline{\text{HOME}}$ line. If a Hard Copy Unit is connected to the Terminal, HOME prevents voltage fluctuations from initiating a hard copy. Pulling the $\overline{\text{HOME}}$ line low resets Terminal logic to the Alpha Mode by inputting to the Graf Flipflop to set $\overline{\text{GRAF}}$ high and $\overline{\text{NOLI}}$ low. $\overline{\text{HOME}}$ also resets the X and Y Registers (in TC-2) to position the writing beam to the Home position (upper-left corner of display screen). After the power stabilizes, the Home circuit is deactivated.

Column Decoder. Basically, the Column Decoder is a binary-to-decimal decoder. The inputs to the Column Decoder are as follows:

1. $\overline{\text{TERMINAL STROBE}}$ ($\overline{\text{TERM STB}}$) from U107B.
2. $\overline{\text{NOLI}}$ from Graf Flipflop.
3. $\overline{\text{BIT 7}}$ from minibus.
4. $\overline{\text{BIT 6}}$ from minibus.

For any of the outputs from the Column Decoder to be active, $\overline{\text{NOLI}}$ and $\overline{\text{TERM STB}}$ must be low. $\overline{\text{TERM STB}}$ goes low when $\overline{\text{TSTROBE}}$ is low if $\overline{\text{BTSUP}}$ and $\overline{\text{TSUP}}$ are high. This allows $\overline{\text{BIT 7}}$ and $\overline{\text{BIT 6}}$ to set the outputs. Referring to the Code Chart in Section 1, it can be seen that $\overline{\text{BIT 6}}$ and $\overline{\text{BIT 7}}$ determine which two columns of the chart are selected for operation.

Refer to Table 6-10. Note that either $\overline{\text{ALPHA STB}}$ or $\overline{\text{CTRL CHAR STB}}$ can be generated with $\overline{\text{NOLI}}$ low. Also note that $\overline{\text{CTRL CHAR STB}}$ can still be generated when $\overline{\text{NOLI}}$ goes high (Graph Mode), but the $\overline{\text{ALPHA STB}}$ signal is replaced by Graph commands $\overline{\text{LOY}}$, $\overline{\text{LOXE}}$, $\overline{\text{HIY}}$, or $\overline{\text{HIX}}$.

TABLE 6-10

Logic Decoder for Column Decoder and Graphic Byte Decoder

INPUT SIGNAL				RESULTANT SIGNAL	COLUMNS OF ASCII CODE CHART
TERM STB	NOLI	BIT 7	BIT 6		
0	0	0	0	ALPHA STB	6 and 7 (LOWER CASE)
0	0	0	1	ALPHA STB	4 and 5 (UPPER CASE)
0	0	1	0	ALPHA STB	2 and 3 (SYMBOLS & NUMERALS)
0	0	1	1	CTRL CHAR STB	0 and 1 (CTRL CHARACTERS)
0	1	0	0	LOY	6 and 7 (5 LSB of Y ADDRESS)
0	1	0	1	LOXE	4 and 5 (5 LSB of X ADDRESS)
0	1	1	0	HIY	2 and 3 (5 MSB of Y ADDRESS)*
				HIX	2 and 3 (5 MSB of X ADDRESS)*
0	1	1	1	CTRL CHAR STB	0 and 1 (CTRL CHARACTERS)

***Preceding signal determines whether HIY or HIX goes active. HIY goes active following a GS or the LOXE signal; HIX goes active following the LOY signal.**

Control Character Decoder. Refer back to Fig. 6-12. The Control Character Decoder consists of two 4-line to 16-line decoders.

As a result of the enabling signals (CTRL CHAR STB and BIT 5) and the data (BIT 1—BIT 4), the Control Character Decoder will output low signals for the following control characters: US, BEL, VT, HT, BS, CR, LF, ENQ, GS, ESC, FF, SUB, ETB, SI, and SO. The control character signals are then processed by the applicable circuitry in TC-1 to perform the desired function. This circuit decodes all 32 ASCII control characters. However, only those mentioned above are used by the Terminal logic.

Escape. Six control characters are dependent upon a preparatory command to arm the circuitry before they can be executed. The preparatory command is Escape (ESC) and the dependent commands are Form Feed (FF, which generates a PAGE signal to erase the display and set the Terminal to Alpha Mode, home position), Substitute (SUB, which initiates the Graph Input Mode and starts the Crosshair Cursor), End of Transmission Block (ETB, which activates the MAKE COPY pulse to turn on the Hard Copy Unit), Inquire (ENQ, which is sent to request Terminal status), Shift Out (SO, which selects the alternate character set if one is installed and the ROM SELECT option strap is at AB+BC), and Shift In (SI, which selects the ASCII character set if the ROM SELECT option strap is at AB+BC). The purpose of the Escape circuitry is to prevent accidental activation of these signals.

Assume that the ESC data bits are placed on the minibus. The Escape circuitry functions in the following manner. With BTSUP and TSUP inactive, TSTROBE (which accompanies the data bits) enables the Column Decoder to generate the CTRL CHAR STB signal. This signal permits the Control Character Decoder to decode BIT 1—BIT 5; the ESC signal goes active and "arms" the Escape Flipflop, setting LCE (Last Character to Escape) high. The arrival of the data bits for the next portion of the two-character sequence activates the required function. ETB activates MAKE COPY; FF activates PAGE; SUB activates CURSE; ENQ activates INQUIRE; SO sets APL high to select the alternate character set; SI sets APL low to select the ASCII character set. The positive-going CLEAR signal from U20A (which occurs whenever TSTROBE ends) disarms the Escape Flipflop unless the ESC character accompanies TSTROBE. Thus, the Escape Flipflop is always disarmed by the character following the ESC input, causing LCE to return low.

Page, Curse, Make Copy, Inquire, and APL. These five circuits comprise an additional portion of the Escape circuitry, and were generally explained under that topic. Some additional comments about the Make Copy circuit follow. The 5 Hz input from the Alpha Cursor Counter controls the width of the MAKE COPY pulse. HOME inhibits the Make Copy circuit when power is turned on. Notice that MAKE COPY inputs to the Terminal Busy circuit. This keeps the Terminal busy (TBUSY goes low) until the Hard Copy Unit asserts DRBUSY to sustain the busy condition. This holds the Terminal in a busy condition from the time MAKE COPY is activated to the time the Hard Copy Unit completes the copy and DRBUSY goes high.

Graf Flipflop. The Graf Flipflop switches the Terminal in and out of Graph Mode. The GS control character sets the Graph Mode. $\overline{\text{NOLI}}$ goes high to enable the Linear Interpolation circuitry in TC-2. $\overline{\text{GRAF}}$ goes low and sets other Terminal circuitry for Graph Mode operation. The signals $\overline{\text{PAGE}}$, $\overline{\text{CURSE}}$, and $\overline{\text{HOME}}$ reset the Graf Flipflop to the Alpha Mode. The control characters US and CR can also reset the Graf Flipflop to the Alpha Mode.

When $\overline{\text{GS}}$ sets $\overline{\text{GRAF}}$ low and $\overline{\text{NOLI}}$ high, $\overline{\text{NOLI}}$ enables the Column Decoder to allow $\overline{\text{BIT 7}}$ and $\overline{\text{BIT 6}}$ to control the Byte Enable lines to the Graphic Byte decoder.

Graphic Byte Decoder. This circuit generates the graphic byte output signals $\overline{\text{HIY}}$, $\overline{\text{LOY}}$, $\overline{\text{HIX}}$, and $\overline{\text{LOXE}}$. These signals are used to load the four graphic bytes into the Data Latches on TC-2. When the Terminal receives graphic plot data, it arrives in a sequence of 4 seven-bit bytes for each coordinate point addressed. Five of the bits contain coordinate information and two of the bits (bits 6 and 7) contain steering data. The steering data designates the specific byte as being either High Order Y (HIY), Low Order Y (LOY), High Order X (HIX), or Low Order X (LOX), received in that order. The Graphic Byte Decoder operates in the following manner.

When the Terminal receives a GS control character, it activates the GS signal from the Control Character Decoder. This signal sets the Graphic Plot Mode as previously explained. With $\overline{\text{NOLI}}$ inactive (high), the Column Decoder will now interpret $\overline{\text{BIT 6}}$ and $\overline{\text{BIT 7}}$ as BYTE ENABLE information for the Graphic Byte Decoder. The graphic byte code bits are as follows:

BYTE	BIT 7	BIT 6	Contents
HI Y	0	1	Most significant 5 bits of Y
LOY	1	1	Least significant 6 bits of Y
HIX	0	1	Most significant 5 bits of X
LOX	1	0	Least significant 5 bits of X

Notice that the HIY and HIX bits have the same bit 7 and bit 6 configuration. The problem of interpreting which byte is which is accomplished by the $\overline{\text{GS}}$ signal, the LOY byte, and the LOX byte. The $\overline{\text{GS}}$ signal sets the Graphic Byte Decoder to interpret the first high order code as being HIY. The LOY code, causes the Graphic Byte Decoder to interpret the next high order code as HIX. Each time a vector is executed by the $\overline{\text{LOXE}}$ signal, the circuit resets to recognize the next high order byte as HIY.

Notice that the $\overline{\text{GIN}}$ signal inputs to the Graphic Byte Decoder. Its purpose is to inhibit the Decoder during the sending of graphic input data to the computer.

Format Effector

General. The Format Effector operates from a predetermined set of inputs to position the Alpha cursor over the face of the display screen. It also generates timing pauses when switching out of graphics, when initiating a Carriage Return, when ringing the bell, and when drawing a vector.

Its basic function is to take the decoded output of the Control Character Decoder and transform it into the desired result. For example, if the function desired is to move the Alpha cursor one space, the Format Effector will output 14 pulses on the $\overline{\text{RIGHT}}$ line. This will increment the X Register in TC-2, thus moving the Alpha cursor one space. Each pulse will increment the X Register one count. Each count from the Register will move the display beam one Tekpoint. (A Tekpoint refers to one of the 1024 programmable locations that are available in both the X and Y Axes.) Another example is a Carriage Return. With a Carriage Return, the Control Character Decoder outputs the $\overline{\text{CR}}$ signal. The Format Effector circuitry inverts the $\overline{\text{CR}}$ to CR, which sets the X Register back to zero. At the same time, the Format Effector generates a pause in Terminal operation, causing the Terminal to go to a "busy" condition. This pause is of sufficient length to allow the display beam to position back to the left side of the screen before the Terminal will accept and process further data.

The Format Effector contains the following circuits:

System Clock—Provides timing signals for Terminal operation.

Alpha Cursor Counter—Controls the positioning of the Alpha cursor as well as various other functions.

Pulse Shaper—Provides a pulse that loads preset data into the Alpha Cursor Counter circuit.

Direction Latch—Remembers the direction of last Alpha cursor movement. Its output changes when new direction command is received.

Direction Enable Gates—Enables $\overline{\text{LEFT}}$, $\overline{\text{RIGHT}}$, $\overline{\text{UP}}$, or $\overline{\text{DOWN}}$ lines dependent upon respective signals from Direction Latches and the enabling signals from the Alpha Cursor Counter.

Terminal Busy—Outputs a $\overline{\text{TBUSY}}$ signal that prevents the Terminal from receiving any further data until the Terminal operation being performed is completed.

Line Feed/Carriage Return (LF/CR)—Performs a line feed upon receipt of an EOL signal. Can be strapped to cause a Carriage Return upon receipt of the LF control character.

Vector/Bell Enable—Outputs signals that activate vector drawing and bell ringing.

Z Axis—Controls the state of the X signal that turns the display beam on and off.

Bell—Provides the drive signal for the speaker that produces the audible "bell" tone.

View/Hold—Provides an enabling signal (VIEW) for the CRT flood guns so that data can be viewed. When in Hold operation, VIEW is set at a reduced duty factor, thus prolonging the life of the CRT.

Cursor Refresher—Provides logic that allows the 7 X 9 dot matrix of the Character Generator to be displayed but not stored, thus generating the Alpha cursor.

Defocus—Provides uniform focusing in Alpha and GIN Modes.

Basically, the operation of the circuits will be described in that order. However, in some cases it is more practical to combine the descriptions of several blocks.

System Clock. The System Clock is a Crystal-Controlled oscillator that outputs two square-wave frequencies to the minibus: 4.9 MHz and 614 kHz. It also outputs a 2.45 MHz square wave for use by the Alpha Cursor Counter and the LF/CR circuit.

Pulse Shaper. The Pulse Shaper generates a $\overline{\text{LOAD}}$ pulse that strobes data from the preset lines into the Alpha Cursor Counter. The $\overline{\text{LOAD}}$ pulse is shorter than any of the inputs to the Pulse Shaper circuit. This allows the $\overline{\text{LOAD}}$ pulse to come and go while the data on the preset lines is still valid. All inputs to the Pulse Shaper will activate the $\overline{\text{LOAD}}$ pulse. The $\overline{\text{LOAD}}$ pulse is inverted and input to the Vector/Bell Enable and Direction Latch circuits as a LOAD signal.

Alpha Cursor Counter, Direction Latch, and Direction Enable Gates. The Alpha Cursor Counter is composed of 4 four-bit counter elements. Depending upon preset inputs to the counter, it will add or subtract the required number of pulses to initiate the function required by the Control Character Decoder. This circuit also generates pauses in Terminal operation, such as that required for a Carriage Return, (as previously explained), and coming out of Graphic operation. It also provides a 2.6 ms pause that activates the $\overline{\text{Z}}$ signal when drawing a vector. Finally, it provides various timing signals that are used by other TC-1 circuits.

The Clock input to the Alpha Cursor Counter is a 2.45 MHz square wave from the System Clock. The Counter counts continuously except when a low is applied on the $\overline{\text{LOAD}}$ input line. As the Counter circuitry is counting, it is putting out the following square-wave signals for use by other TC-1 circuits:

5 Hz. Used in the Cursor Refresher circuit and Make Copy circuit.

37 Hz. Used in the Cursor Refresher circuit.

75 Hz, 150 Hz, 300 Hz. Used in the View/Hold circuit.

1200 Hz. Used in the Bell circuit.

153 kHz. Used by the Character Generator.

1.25 MHz. Used to increment the Direction Enable Gates and to clear the Column Reset circuitry located in the Character Generator circuitry.

The Alpha Cursor Counter is a programmable counter, referred to as such because it contains a number of preset lines that "program" the Alpha Cursor Counter to output various signals that perform a specific function. The data loaded into the Counter from the preset lines determines a number that the Counter will start counting from. These preset inputs are: $\overline{\text{LOXE}}$ (Low Order X Enable), which sets the 2.6 ms pause that activates the $\overline{\text{Z}}$ signal to draw a vector; the Bell input that determines how long the bell will ring; the $\overline{\text{CR}}$ input that initiates the pause needed to perform the Carriage Return; and finally $\overline{\text{BS}}$ (Backspace), $\overline{\text{HT}}$ (Horizontal Tab), $\overline{\text{VT}}$ (Vertical Tab), and $\overline{\text{LF}}$ (Line Feed). Notice that the same preset line is used for both directions of horizontal movement; similarly, one preset line is used for both directions of vertical movement. This is because for either a BS or an HT, the horizontal movement is 14 Tekpoints. For either a VT or an LF, the vertical

movement is 22 Tekpoints. Each of the eight functions the Counter will perform corresponds to a definite value on the preset input lines. These lines determine how long it will take for the Counter to count up to the point where a zero-to-one transition is obtained on its Most Significant Bit (MSB) output. If either a LEFT, RIGHT, UP, or DOWN signal is being output by the Direction Latch, this length of time determines how many 1.25 MHz pulses are placed on the $\overline{\text{LEFT}}$, $\overline{\text{RIGHT}}$, $\overline{\text{UP}}$, or $\overline{\text{DOWN}}$ line, as well as how long $\overline{\text{TBUSY}}$ stays active. In all cases, the MSB signal being low determines how long it will take for a Terminal pause, as reflected by the $\overline{\text{TBUSY}}$ signal.

For an example of how the Format Effector processes a direction command, assume that Control Character HT (space) has been received by the Terminal. $\overline{\text{HT}}$ inputs to the Pulse Shaper circuit and causes the $\overline{\text{LOAD}}$ pulse to go low. LOAD then strobes the $\overline{\text{HT}}$ signal into the Direction Latch, activating the RIGHT signal; $\overline{\text{LOAD}}$ simultaneously loads the preset data into the Alpha Cursor Counter, causing the MSB signal to go low. With MSB low, $\overline{\text{TBUSY}}$ goes active and the 1.25 MHz signal clocks the Direction Enable Gates. With the RIGHT signal from the Direction Latch high, every time the 1.25 MHz signal goes low, a low-going transition takes place on the $\overline{\text{RIGHT}}$ line, incrementing the X Register in TC-2. After 14 positive-to-negative transitions of the 1.25 MHz signal, the MSB signal goes high. This prevents the 1.25 MHz signal from enabling further $\overline{\text{RIGHT}}$ pulses. It also ends the $\overline{\text{TBUSY}}$ signal.

The $\overline{\text{FPAUSE}}$ signal is an output of TC-2. Its purpose is to disable the Alpha Cursor Counter circuit when the X Register in TC-2 resets from 1023 back to 0. Here it is used to generate the pause required for proper operation of the LF/CR circuit when used with a clocked interface. It does not cause the MSB signal to go low. It simply stops the counting sequence for approximately 0.5 ms.

Terminal Busy. The Terminal Busy circuit inhibits the reception of data from either the keyboard or the computer. Any of the following functions will cause $\overline{\text{TBUSY}}$ to go active low: when an alphanumeric character is being generated ($\overline{\text{CHAR IN PROG}}$); when a Hard Copy is being generated ($\overline{\text{MAKE COPY}}$ and $\overline{\text{DRBUSY}}$); and when the Most Significant Bit (MSB) output of the Alpha Cursor Counter is low.

Automatic Carriage Return/Line Feed. When the Control Character Decoder outputs an $\overline{\text{LF}}$ signal, the Auto CR/LF circuit will, in turn, output an $\overline{\text{LF}}$ signal to the Pulse Shaper and Direction Latch circuits to cause the Line Feed to occur. Notice that the control character signal $\overline{\text{CR}}$ also inputs to this circuit. This signal is inverted and outputs on the CR line. The Auto CR/LF circuit can be strapped (see Strappable Options section of the manual) to generate both an LF and a CR signal when $\overline{\text{LF}}$ goes active.

The $\overline{\text{EOL}}$ (End of Line) input (from TC-2) activates a line feed and a carriage return when spacing past the end of the line. An active SUPPRESS signal from the Alpha Cursor Suppress circuit inhibits the operation of the automatic CR/LF circuit during Graph and GIN Modes.

Vector Bell Enable. When the control character $\overline{\text{BEL}}$ goes low, it enters the Pulse Shaper to generate the $\overline{\text{LOAD}}$ pulse. $\overline{\text{BEL}}$ then gets strobed into the Vector/Bell Enable circuit by the LOAD pulse. The circuit then outputs BELL and $\overline{\text{BELL}}$ to generate the bell tone. For more on how the Bell circuit works, see the explanation on the Bell circuit. This circuit is also used to enable or disable the Z axis during the drawing of a vector (Linear Interpolation). It functions in the following manner.

Circuitry within the Vector/Bell Enable circuit keeps the VECTOR ENABLE signal to U253B low for the first vector following GS. This is known as a "Dark Vector". With the receipt of the next vector, the $\overline{\text{LOXE}}$ signal causes the Vector/Bell Enable circuit to set the VECTOR ENABLE signal high. VECTOR ENABLE provides an enabling voltage to one side of Vector Enable Gate U253B. The $\overline{\text{LOXE}}$ signal also inputs to the Alpha Cursor Counter to preset the inputs for a 2.6 ms pause. The $\overline{\text{LOAD}}$ signal then sets the 2.6 ms PAUSE line to U253B high. U253B is now enabled and sends a low $\overline{\text{DRAW}}$ signal to the Z Axis circuit. This action sets the $\overline{\text{Z}}$ signal low to draw the vector. 2.6 ms later, the 2.6 ms PAUSE line goes low, disabling the Z Axis circuit.

Z Axis. The Z Axis circuitry enables or disables the $\overline{\text{Z}}$ signal. $\overline{\text{Z}}$ is an active low signal that is used to turn the writing beam on. The effect that $\overline{\text{DRAW}}$, $\overline{\text{TOP ROW SUPPRESS}}$, $\overline{\text{WRITE DOT}}$, and $\overline{\text{REFRESH}}$ have upon Z Axis operation is described in the block from which they originate.

Bell. When the control character BEL is received, $\overline{\text{BEL}}$ goes low from the Control Character Decoder. $\overline{\text{BEL}}$ inputs to the Pulse Shaper circuit to generate a $\overline{\text{LOAD}}$ pulse that is inverted to latch $\overline{\text{BEL}}$ into the Vector/Bell Enable circuit. This causes the BELL and $\overline{\text{BELL}}$ signals to go high and low respectively. While the $\overline{\text{LOAD}}$ pulse is active low, it latches

the BELL and $\overline{\text{BELL}}$ inputs to the Alpha Cursor Counter and the Counter starts counting. The $\overline{\text{LOAD}}$ pulse also causes the MSB output of the Counter to go low. This low MSB signal with the high $\overline{\text{BELL}}$ signal from the Vector/Bell Enable circuit allows the 1200 Hz square-wave signal to drive the Bell circuit, thus generating 1200 Hz tone. When the Counter counts up to the point where the MSB goes high (as determined by the preset input from the Vector/Bell Enable circuit) the Bell circuit is disabled.

View/Hold. The purpose of the View/Hold circuit is to prolong the life of the display tube. In the Alpha Mode, as long as data is being entered into the Terminal, the VIEW signal is high, allowing data to be displayed. However, if no new data is entered for a period of about 90 seconds, the VIEW signal becomes modulated by a 75 Hz signal from the Alpha Cursor Counter. This action provides a 12 1/2% duty time for the VIEW signal, thus dimming the display. This is known as "Hold" status. The display can be returned to normal viewing level by entering new data, or by pressing the SHIFT key. The input signals must be in the following states before Hold status can occur.

1. SUPPRESS—Low
2. $\overline{\text{HOME}}$—High
3. $\overline{\text{SHIFT}}$—High

Notice that this circuit inputs a signal called $\overline{\text{VIEW}}$ to the Cursor Refresher circuit. When the 90 second period occurs, this signal goes low to inhibit the Alpha cursor during the time the Terminal is in Hold.

If either the $\overline{\text{GRAF}}$, $\overline{\text{GIN}}$, $\overline{\text{DRBUSY}}$, or $\overline{\text{TERM STB}}$ signals go active, the SUPPRESS signal from the Alpha Cursor Suppress circuit goes high. This keeps the view signal active.

Cursor Refresher. The Alpha cursor is a pulsating display of a 7 X 9 dot matrix. When the Terminal is in the Alpha Mode, the Character Generator continuously cycles through the character dot matrix at an approximate 1200 Hz rate. If no character is being written, the CURSOR INH signal goes low, enabling the Cursor Refresher circuit. If VIEW is high, the 5 Hz, 38 Hz, and 154 kHz signals combine to provide enabling pulses on the REFRESH line, which causes Z signals to produce a pulsating, non-storing cursor. The 5 Hz combines with the 38 Hz and the CARRY signal to produce the pulsation; the 154 kHz clock provides the REFRESH signals. The CURSOR INH signal disables the circuit during Graph and GIN Modes.

When a character is to be written, $\overline{\text{TERM STB}}$ initially disables the Cursor Refresher circuit; this is reinforced by the CURSOR INH signal going high and remaining high until character writing is completed and $\overline{\text{TBUSY}}$ returns high.

A conceptual drawing of the $\overline{\text{Z}}$ output pulses during Alpha cursor writing appears in Fig. 6-13.

Defocus. The Defocus circuit generates the $\overline{\text{FUZZ}}$ signal, which goes high during character generation and Graph Mode to provide optimum focus. In GIN Mode, and during Alpha cursor generation, $\overline{\text{FUZZ}}$ goes low to provide focus control of the crosshair and Alpha cursors, independent of character and vector focus.

Character Generator

General. The Character Generator performs several operations during character writing to provide the display screen with necessary information. The principal operations are:

1. Sequentially place the writing beam to each of 16 vertical positions (rows) in each of 8 horizontal positions (columns) to form a 9Y by 7X matrix for character writing. See Fig. 6-14.

2. Examine the Read Only Memory circuits at each position to see if a dot is to be written. (The dot information is dependent upon the character being executed.)

3. Turn the writing beam on at positions indicated by the ROM. The combination of written dots forms the character being written. See Fig. 6-14.

4. Generate a busy signal until character writing is complete.

5. Shift the matrix position up or down (or leave it unshifted) as required by the character being written. Generally the operation is performed in the following manner. Refer to Figs. 6-12 and 6-15 as necessary.

(1) A writing character is strobed into the circuit.

(2) The circuit is preset to its starting point (row Ø column Ø). The dot information for column Ø, rows 7 through 15 is made available to the Dot Multiplexer on 9 separate lines. The Character Modifier circuit takes note of the shift information from the ROM. If the line is high, it indicates either a normal or subscript character. If the line is low, it indicates superscript or italics. Column 1 must be examined before final determination can be made, so the column Ø shift information is stored in a memory circuit.

(3) The Row Counter steps through the 16 rows. Since no dot information ever appears in column Ø, no dots are written.

(4) The Column Counter shifts to column 1 and the X Axis is deflected to the next column. Its dot information is made available to the Dot Multiplexer on the row 7 through row 15 lines. The column 1 shift information is also made available to the Character Modifier. If a high signal exists, it indicates either a normal or italic character; if low, it indicates either a superscript or a subscript. This is compared against the column Ø memory and the circuit is influenced accordingly. (If column Ø says normal or subscript and column 1 says normal or italic, normal prevails.)

(5) The Row Counter steps through from row Ø to row 6 while the circuitry settles. Although beam deflection takes place, no dot writing can occur, since beam unblanking is inhibited. The Row Counter continues to step through row 7 through row 15. If any dots are indicated by the row 7 through 15 lines from the ROM, they permit a dot to be written when the counter reaches their position.

(6) After stepping through column 1 row 15, the Column Counter is advanced to column 2 and the Row Counter to row Ø. Column 2 dot information is now made available on the row 7 through 15 lines from the ROM, and shift information continues to be made available to the Character Modifier circuit. (The column 2 shift information is always the same as the column 1 shift information, as is the shift information in columns 3 through 7.)

(7) The operation continues in like manner, stepping through all columns until column 7 has been scanned and writing is complete.

(8) The Cursor Refresh circuit then becomes enabled. The Column and Row Counters continue to cycle, and each dot in row 7 through 15 of column 1 through 7 is written (as previously described) until another writing character is received, or Hold status occurs, or another operating mode is selected.

The following principle circuits make up the Character Generator.

ROM A, ROM B, ROM C—The ROM selected can be one of three Read Only Memory devices. ROM A and ROM B can provide character writing information for all writing characters in the ASCII code. The selected ROM is programmed by the character being processed ($\overline{\text{BIT 1}}$–$\overline{\text{BIT 7}}$).

ROM Selector—Selects either ROM A, ROM B, or ROM C.

Character Status—Activates the generation of a character. Sets $\overline{\text{TBUSY}}$ active; completes the character generation process by sending a signal to the Format Effector to space to the next character position.

ROW Counter—Cycles through 16 binary counts at each column selection; its output causes the CRT beam to deflect in the Y direction; it also causes the ROM Dot Multiplexer to sequentially examine the dot writing information being emitted by the selected ROM.

Column Counter—Sequentially selects column 0 through 7, causing the CRT beam to deflect in the X direction; selects the appropriate column information from the selected ROM.

Character Modifier—Provides character modifying signals to the X Mat Digital-to-Analog and Y Mat Digital-to-Analog circuits to establish normal italics, subscript, or superscript writing.

Write Dot—Provides write dot information pulses to control the Z Axis circuit.

Dot Multiplexer—Sequentially examines the dot information from the ROM as the Row Counter steps through the rows. The output state is dependent upon the ROM outputs and controls the Z Axis writing via the Write Dot circuit.

Alpha Cursor Suppress—Suppresses character generation during Graph Mode, during Hard Copy operation, etc.

Character Latches—Latches character bits into the Character Generator.

Y Matrix Digital-to-Analog—Converts the digital output of the Row Counter into its analog equivalent for display beam positioning.

X Matrix Digital-to-Analog—Converts the digital output of the Column Counter into its equivalent analog voltage for display beam positioning.

Column Reset—Resets the Column Counter to column 0 of the character matrix.

GIN Echoplex Suppression—Inhibits character generation.

Selecting the ROM. The Character Generator produces the full ASCII writing character set by using two selectable Read Only Memory (ROM) devices, ROM A and ROM B. If a third ROM (ROM C) is installed to produce an alternate character set, it can also be selected if the ROM SELECT option strap is at AB+BC.

Refer to the TC-1 Block Diagram. Four inputs to the ROM Selector control ROM selection by sending a high to enable the desired ROM. The input signals are $\overline{\text{CIP}}$ (Character In Progress), BIT 6, BIT 7 and APL, and they control selection in accordance with Table 6-11.

TABLE 6-11

ROM SELECTOR TRUTH TABLE

INPUTS				ROM SELECTED		
$\overline{\text{CIP}}$	APL	BIT 7	BIT 6	ROM A	ROM B	ROM C
0	0	0	0	0	0	0
0	0	0	1	1	0	0
0	0	1	0	1	0	0
0	0	1	1	0	1	0
0	1	0	0	0	0	0
0	1	0	1	0	0	1
0	1	1	0	0	1	0
0	1	1	1	0	0	1
1	0	0	0	0	0	0

Note that ROM selection is inhibited when the most significant input ($\overline{\text{CIP}}$) is high (inactive). $\overline{\text{CIP}}$ enables the ROM selector only when a character is being generated, enabling ROM selection in accordance with the three least significant inputs.

Presetting the Character Generator. When the data bits for a character are received by the Terminal, $\overline{\text{TSTROBE}}$ activates the $\overline{\text{TERM STB}}$ signal. $\overline{\text{TERM STB}}$ causes the Column Reset circuit to output a $\overline{\text{COLUMN RESET}}$ pulse that sets the Column Counter to zero.

When $\overline{\text{TERM STB}}$ goes active, it causes the Column Decoder to output an active $\overline{\text{ALPHA STB}}$ signal. This signal loads $\overline{\text{BIT 1}}$–$\overline{\text{BIT 7}}$ into the Data Latches to make them available to the Character Generator circuitry. $\overline{\text{ALPHA STB}}$ also causes the Character Status circuit to set the $\overline{\text{CIP}}$ signal active. Its complement, CIP, goes high and enters the Character Modifier and Write Dot circuits. With $\overline{\text{CIP}}$ active, the ROM Selector can select the appropriate ROM device as per the APL, BIT 6 and BIT 7 inputs. $\overline{\text{CIP}}$ also enters the Terminal Busy circuit, causing $\overline{\text{TBUSY}}$ to remain active during the writing of a character (approximately 860 microseconds).

Notice that the $\overline{\text{ALPHA STB}}$ signal enters the Row Counter circuit. In this circuit it provides a clear function, setting the BCD outputs of the Row Counter low. The low-going outputs of the Row Counter cause the Address Read (AR) signal to go active. AR causes the output of the Column Counter to be loaded into the ROMs, selecting the column Ø dot information. The low-going outputs of the Row Counter also cause the Y MAT signal to deflect the writing beam up to the top of the matrix.

When $\overline{\text{TSTROBE}}$ ends, so does $\overline{\text{TERM STB}}$ and $\overline{\text{ALPHA STB}}$. The next negative-going edge of the 1.25 MHz square wave causes the Column Reset signal to go inactive. The Row Counter circuit begins counting on the next trailing edge of the 154 kHz clock pulse.

Scanning the Character Matrix. After the Row Counter outputs are cleared to zero and $\overline{\text{ALPHA STB}}$ goes inactive, the Row Counter can begin counting. The Row Counter counts 7 consecutive times before the Z Multiplexer begins sampling dot information contained in the ROMs. (No Write Dot information is contained in column Ø.) The seventh through fifteenth counts result in the Z Multiplexer's sampling the dot information for each row in the writing matrix.

After the Row Counter clocks through the nine dot positions of the first column, the next 153 kHz clock pulse causes the Row Counter outputs to once again go low, setting the Y MAT signal to row Ø position. The low-going edge of the ÷8 output clocks the Column Counter, causing

its output to select column 1 of the addressed character. The X Matrix Digital-to-Analog circuit output (X MAT) changes to reflect the beam's new horizontal position. When the outputs of the Row Counter went low, they caused the output of the Y Matrix Digital-to-Analog to shift the writing beam up to row Ø position. However, because of the frequency response of the beam deflection circuits, the writing beam cannot position from the bottom of one column to the top of the next column as rapidly as the Counters can indicate this new position. Therefore, beam settling time is provided by not using row Ø through 6 for dot writing. Row 7 through 15 selection cause the Multiplexer to examine the dot information from the ROMs as before. Since column 1 is now selected, dot writing commands can be expected for any character writing that requires a dot (or dots) in column 1. (See Fig. 6-15.) The $\overline{\text{FUZZ}}$ and CIP signals enable the Write Dot circuit during character writing.

The 154 kHz clock negative edge that causes row counting also starts a Multivibrator in the Write Dot circuit. The Multivibrator output pulse duration can be adjusted by R74 Character Brightness, and performs two functions. It allows the circuitry to settle down while and after the Row Counter moves to a new row, and controls dot writing time. If the multiplexer discloses that a dot is to be written, a Write Dot pulse is sent to the Z Axis circuit, ending on the next negative transition of the 154 kHz clock.

Refer once again to Fig. 6-15 and notice that the letter "L" is shown in the matrix. Nine clock pulses provide nine successive $\overline{\text{WRITE DOT}}$ pulses to the Z Axis circuit when scanning column 1. The Z Axis signal is turned on and off to write the dots as the Row Counter steps through all rows in column 1, with the Y MAT changing the beam to each new position.

When the row count once again switches from 15 to Ø, the ÷8 line once again clocks the Column Counter, causing its output to indicate column 2. The new column code, in combination with the active AR signal, selects column 2 dot information from the ROM. The scanning sequence repeats itself until all seven columns of the character have been scanned and the remaining Character dots written.

Resetting the Character Generator. When the Row Counter counts past the row 1 dot of column 7, the low-going ÷8 line clocks the Column Counter once more. This time, the column outputs (÷1, ÷2, ÷4) go low, and a signal called CARRY goes high. CARRY actually signifies a binary count of 9 from the Column Counter. It inputs to the Character Status circuit to generate the $\overline{\text{CHAR COMP}}$ (Character Complete) signal. $\overline{\text{CHAR COMP}}$ enters the Pulse Shaper circuit, where it causes the Format Effector circuitry to advance the display beam one character space.

The CARRY signal also enters the Column Reset circuit. Here it causes the COLUMN RESET signal to go active on the next trailing edge of the 1.25 MHz clock. $\overline{\text{COLUMN RESET}}$ clears the Column Counter, terminating the CARRY signal. When CARRY goes low, $\overline{\text{CIP}}$ (that is holding the Terminal busy) ends. Its complement (CIP) also ends, inhibiting the Write Dot circuitry. The $\overline{\text{CHAR COMP}}$ signal also ends, completing the resetting of the Character Generator.

GIN Echoplex Suppress Circuit. When either the GIN or the Graph Mode is selected, the output of the Echoplex Suppress circuit becomes active. Its purpose is to prevent the Character Status circuit from responding to the $\overline{\text{ALPHA STB}}$ signal. In GIN and Graph Modes, data is used to indicate either writing beam position, Terminal status, or beam addressing information. The Character Generator must not respond to this data that is placed on the minibus. Therefore, when $\overline{\text{GIN}}$ goes active (and notice that $\overline{\text{GS}}$, which sets the Graph Mode, also pulls this line low) a low $\overline{\text{C G SUP}}$ (Character Generator Suppress) signal prevents the Character Status circuit from responding to $\overline{\text{ALPHA STB}}$ signals. This action prevents the Character Generator from responding to the data that generated the $\overline{\text{ALPHA STB}}$ signal. The $\overline{\text{C G SUP}}$ signal also inputs to the Character Modifier circuit, where it causes the CURSOR INH signal to go high. CURSOR INH prevents the Cursor Refresher circuit from refreshing the Alpha cursor during the time that $\overline{\text{C G SUP}}$ is active.

The GIN Echoplex Suppress circuit is reset by the $\overline{\text{LOCAL}}$ and $\overline{\text{TBUSY}}$ signals. $\overline{\text{LOCAL}}$ goes active when the LOCAL/LINE switch is placed in the LOCAL position. $\overline{\text{TBUSY}}$ allows the Character Generator to switch back to alphanumeric character generation when switching out of Graph or GIN Mode. $\overline{\text{TBUSY}}$ occurs automatically when switching from Graph to Alpha Mode. However, $\overline{\text{TBUSY}}$ does not automatically occur when GIN Mode ends, and must be made to occur as explained in the operation information in this manual.

Rubout Detector Circuit. When the data input lines contain the code for the Rubout (DEL) character, the Rubout Detector activates a low-going $\overline{\text{SUP DEL}}$ (Suppress Delete) signal. $\overline{\text{SUP DEL}}$ inhibits the $\overline{\text{CHAR COMP}}$ output of the Character Status circuit. This prevents the Format

Effector from spacing to the next character space when the Delete character is detected.

Character Generator Suppress in Graph Mode. During Graph Mode, or when making a copy of the display, the SUPPRESS signal is active. It loads preset inputs into the Row and Column Counters. The Preset input for the Row Counter is +5 VDC; for the Column Counter, it is Ground. These inputs cause the outputs of the two counters to indicate the bottom left corner of the character matrix. Thus, in Graphic Plot Mode, or when making a hard copy of the display, the writing beam is positioned to the lower-left corner of the matrix.

Character Modifier Circuit. This circuit generates the following X and Y Digital-to-Analog Matrix modifier signals: SUB (for Subscript), $\overline{\text{SUP}}$ (for Superscript), and $\overline{\text{ITAL}}$ (for Italics). These signals are dependent on the $\overline{\text{DOT}}$ shift information from the selected ROM, which is, in turn, dependent upon the Character Input.

The Character Modifier circuit becomes enabled by the $\overline{\text{CIP}}$ signal from the Character Status circuit. Its complement, CIP, clears the outputs of the Character Modifier so that each new character received can determine the output.

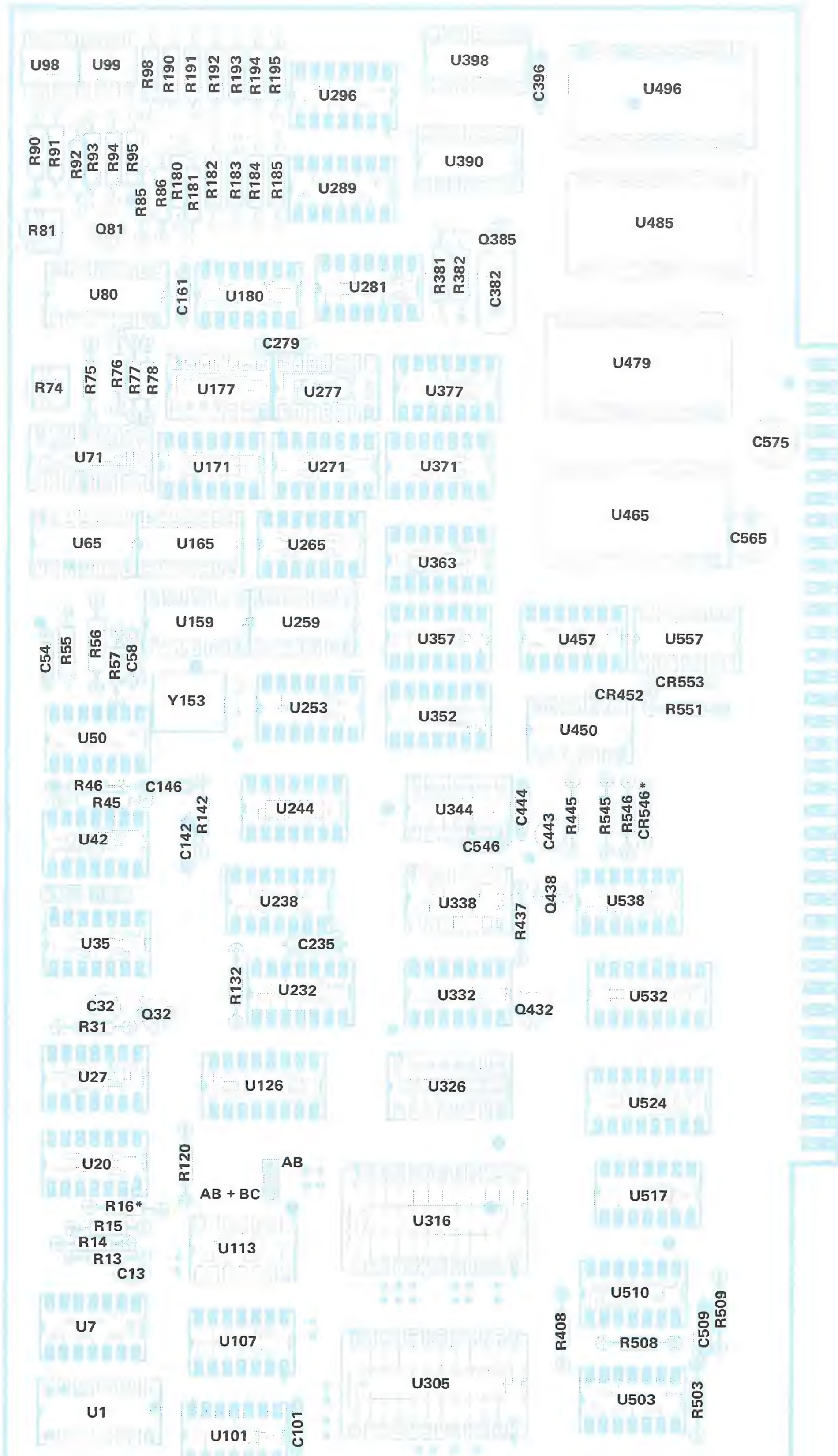
When a character is received and the Column Counter is cleared by the $\overline{\text{COLUMN RESET}}$ signal, the Character Modifier senses the low state of the ÷1, ÷2, ÷4 output lines of the Column Counter. When Row 8 is reached by the Row Counter, the positive going ÷8 output of the Row Counter (in conjunction with the column Ø detected output of the Column Counter) clocks the column Ø Shift Information into a memory in the Character Modifier circuit. When column Ø is completely scanned, the ÷8 output from the Row Counter clocks the Column Counter, addressing column 1. The column 1 shift information from the ROM is immediately felt at the Character Modifier input, where it is compared against the stored column Ø shift information. The comparison results in an output on the SUB, $\overline{\text{SUP}}$, or $\overline{\text{ITAL}}$ line if shifting is to occur, or it results in those three lines remaining inactive if no shifting is indicated. The shift information in Column 2 through 7 is identical to the column 1 shift information, maintaining the same shift instructions throughout writing of a character. The combination of shift information signals required to activate the various shift conditions are as shown in Table 6-12.

TABLE 6-12

Writing Selection

Column 0 Shift Info.	Columns 1—7 Shift Info.	Signal Activated	Writing Selected
LOW	LOW	$\overline{\text{SUP}}$	Superscript
LOW	HIGH	$\overline{\text{ITAL}}$	Italics
HIGH	LOW	SUB	Subscript
HIGH	HIGH	Normal	Normal

$\overline{\text{SUP}}$ goes true if an alternate character set is installed, selected, and requires the matrix to shift up. $\overline{\text{ITAL}}$ goes true if an alternate character set is installed, selected, and requires italic character writing. The $\overline{\text{ITAL}}$ signal combines with a sampling of the Y MAT output to "twist" the X MAT output; thus providing an italic appearance. SUB goes true whenever ASCII lower-case characters g, j, p, q, and y are detected. It causes the Y MAT signal to shift the writing matrix down slightly, writing the tails of the characters below the alphanumeric baseline.



*Present only on cards #670-2667-02 and above

Fig. 6-16. TC-1 Component Locations.

Ⓐ

CKT NO	GRID LOC
CAPS	
C13	D3
C32	C3
C54	D2
C58	B2
C101	B1
C142	B1
C146	B2
C161	B1
C235	C3
C279	G5
C382	F5
C396	B1
C443	D4
C444	C6
C509	B1
C546	D3
C565	B1
C575	B1
DIODES	
CR452	C5
CR553	C5
TRANSISTORS	
Q32	C3
Q81	J5
	I5
Q385	F5
Q432	C6
Q438	D4
RESISTORS	
R13	D3
R14	E2
R15	E2
R31	C3
R45	B2
R46	B2
R55	B3
R56	B2
R57	B2
R74	F5
R75	E2
R76	D2
R77	C5
R78	F5
R81	C5
R85	J5
R86	I5
R90	H6
R91	H6
R92	H6
R93	I5
R94	I5
R95	J5
R98	I6
R120	F2
R132	C3
R142	E2

CKT NO	GRID LOC
RESISTORS	
R180	I5
R181	I5
R182	I5
R183	I5
R184	I5
R185	I5
R190	H6
R191	I5
R192	H5
R193	I5
R194	H5
R195	I5
R381	F5
R382	F5
R408	F3
R437	C6
R445	D4
R503	D6
R508	E2
R509	B2
R545	D4
R546	D4
R551	C6
IC's	
U1A	C3
U1B	C4
U7A	
U7B	D3
U7C	D3
U7D	D3
U7E	D3
U7F	D3
U20A	E1
U20B	E2
U20C	D2
U20D	C2
U27A	H2
U27B	C5
U35A	B3
U35B	B3
U35C	D4
U35D	B3
U42A	B3
U42B	C5
U50A	B2
U50B	B2
U50C	D2
U50D	I2
U50E	I4
U50F	G6
U65	C4
U71A	
U71B	E5
U80	F3
	G3
U98	H6
U99	I5
U101	D2
U107A	F3
U107B	F2
U107C	F3

CKT NO	GRID LOC
IC's (CONT)	
U113A	F3
U113B	F3
U113C	E2
U113D	E2
U126A	C4
U126B	H2
U159	C4
U165	C4
U171A	D5
U171B	D5
U177	D5
U180A	F3
U180B	F3
U180C	G3
U180D	E2
U232A	E2
U232B	E3
U232C	D5
U238A	C3
U238B	C3
U238C	C3
U238D	H2
U244A	C3
U244B	D3
U253A	I2
C253B	C5
U253C	D5
U259	C5
U265B	D4
U265C	I3
U265D	I4
U271A	D5
U271B	D2
U271C	J3
U271D	D5
U277	G5
U281A	J3
U281B	G5
U289A	H3
U289B	G3
U289C	H3
U289D	I3
U289E	I3
U289F	I3
U296A	H5
U296B	
U296C	G5
U296D	H5
U296E	H5
U296F	I5
U305	C2
U316	D2
U326	F2
U332A	C5
U332B	C4
U332C	B5
U332D	D3
U338A	B6
U338B	B6
U338C	B6
U338D	B6
U344	D4
U352A	B5

CKT NO	GRID LOC
IC's (CONT)	
U352B	D3
U357	I3
U363A	C5
U363B	J4
U371A	E2
U371B	J4
U371C	I4
U371D	I2
U377A	G6
U377B	I2
U377C	D6
U390	I3
U398	G5
U450A	B6
U450B	D2
U450C	C2
U450D	D6
U457A	G3
U457B	G3
U457C	D2
U457D	G3
U457E	G3
U457F	G3
U465	G4
U479	H4
U485	H4
	I4
U496	G5
	H5
U503A	D2
U503B	C2
U503C	F2
U503D	G2
U503E	B2
U503F	F3
U510A	
U510B	C1
U517	C3
U524	G2
U532	B4
U538A	B2
U538B	B4
U538C	C5
U538D	B3
U557	I5
CRYSTAL	
Y153	B2

Ⓐ

TC-1 Semiconductor Information

NUMBER	VCC	GND	UNUSED INPUTS
7400	14	7	HIGH
7401	14	7	HIGH
7402	14	7	LOW
7404	14	7	
7408	14	7	LOW
7410	14	7	HIGH
7412	14	7	HIGH
7416	14	7	
7417	14	7	
7420	14	7	HIGH
7425	16	8	LOW
7426	14	7	HIGH
7430	14	7	HIGH
7437	14	7	HIGH
7438	14	7	HIGH
7442	16	8	
7473	4	11	HIGH
7474	14	7	HIGH
7475	5	12	HIGH
7476	5	13	HIGH
7493	5	10	LOW
74111	16	8	HIGH
74121	14	7	HIGH
74122	14	7	HIGH
74145	16	8	LOW
74150	24	12	
74154	24	12	LOW
74197	14	7	

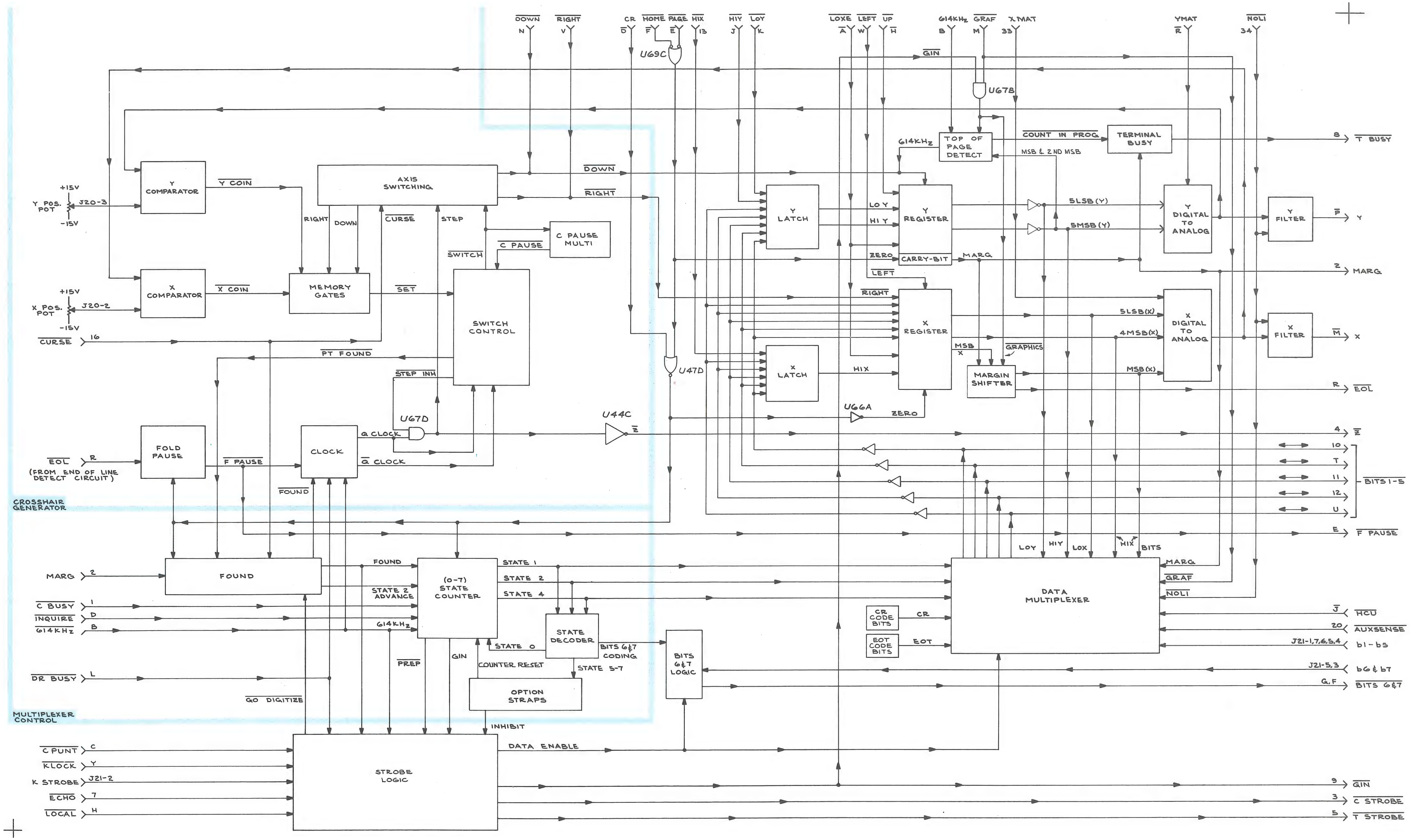
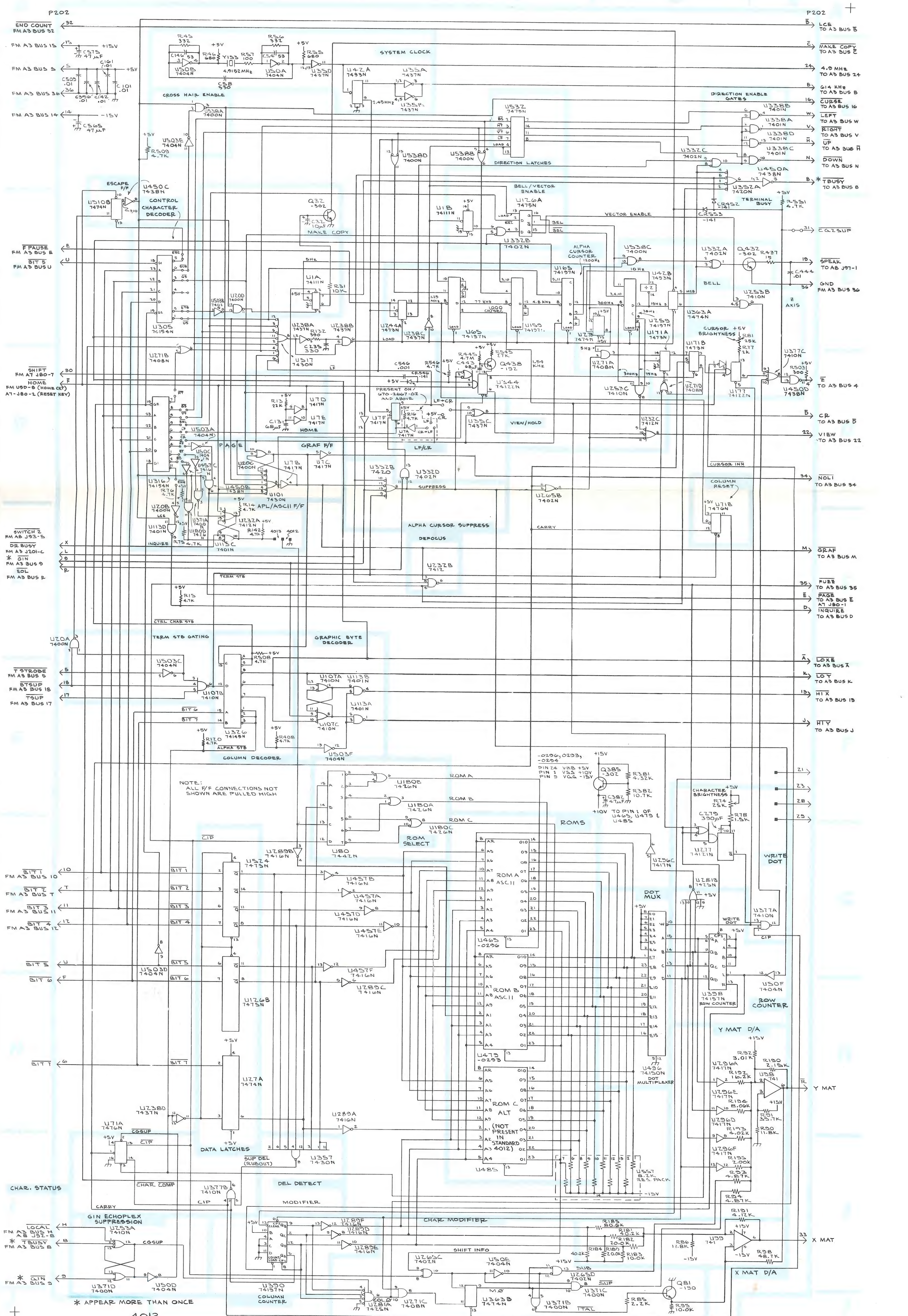


FIG. 6-18 TC-2 DETAILED BLOCK DIAGRAM



4012

A1-TC-1 CIRCUIT CARD

FIG 6-17

TC-1

TC-2 BLOCK DIAGRAM DESCRIPTION

Introduction

Refer to Fig. 6-18. As in the case of TC-1, TC-2 can be divided into blocks that perform specific functions. When possible, each block will be described as a separate entity. However, in some cases, it is difficult to obtain an over-view of circuit operation by discussing an individual block; in such cases, groups of blocks are described in a sequence of operations (such as those needed to generate the crosshair cursor).

Below is a list of blocks that contain the greater part of TC-2 circuitry. A short description of each is given.

X Latch, Y Latch—data latches used when operating in the Graphic Plot Mode; provide storage for three 5-bit bytes of the 20-bit coordinate address.

X and Y Registers—each register contains three 4-bit up-down counters, whose 10 bits of output data can be set by serial or parallel inputs.

Top-of-Page Detect Circuit—in the Alpha Mode, this circuit keeps the display beam in the viewable area of the Y Axis.

Margin Shifter—sets Margin Ø (left side of Display) or Margin 1 (center of Display).

Terminal Busy—places the Terminal in a "busy" condition, inhibiting the placing of data on the minibus by the keyboard, computer, or any other device that might be connected to the minibus.

X and Y Digital-to-Analog (D/A) Circuits—convert the digital outputs of the X and Y Registers into their equivalent analog voltage.

X and Y Filters—in the Graphic Plot Mode, these circuits provide a linear rate of change for the X and Y signals. These circuits have no effect on the D/A outputs in Alpha Mode.

Data Multiplexer—depending upon the output of the Multiplexer Control circuit, the Data Multiplexer will place one of eight data bytes onto the minibus.

Strobe Logic—provides a signal that enables the Data Multiplexer to place the data bytes onto the minibus; also provides strobe signals to enable the computer and/or the Terminal to accept and process data.

Bits 6 and 7 Logic—places the complement of keyboard bits 6 and 7 onto their respective minibus data lines; also codes $\overline{\text{BIT 6}}$ and $\overline{\text{BIT 7}}$ with each 5-bit byte of data from the Data Multiplexer when operating in the GIN Mode.

Multiplexer Control—controls the output of the Data Multiplexer; also inputs various signals to the Strobe Logic circuit to aid in the generation of the strobe signals, and aid in the digitization of the voltage from the X and Y Position Pots.

Crosshair Generator Circuitry—generates the crosshair cursor by sending a sequence of pulses that increment the X and Y Registers. With each register increment, a Z Axis pulse is generated to draw the point. Rapidly counting through the Registers provides a crosshair-type cursor, bright enough to be visible, yet dim enough so as not to store.

Z Control Circuit—(Circuit Cards 670-1729-04 and above)—Controls vector intensity when vectors less than approximately one-half inch long are being drawn.

Block Description

X and Y Data Latches. The X Latch and Y Latch are used in the Graph Mode to provide storage for three of the 5-bit coordinate address bytes. In this mode of operation, data is sent from the computer to draw graphics, charts, figures, etc. on the Display screen. It takes twenty bits of data to establish a new coordinate address. However, only seven bits of data are accepted from the computer at any one time; therefore each coordinate address is divided into 4 seven-bit bytes. Two of the bits contain code data, and are used to develop load signals ($\overline{\text{HIY}}$, $\overline{\text{LOY}}$, $\overline{\text{HIX}}$, and $\overline{\text{LOXE}}$) on TC-1. The $\overline{\text{HIY}}$, $\overline{\text{LOY}}$, and $\overline{\text{HIX}}$ signals load their respective 5 bits of coordinate data into the appropriate Y or X latches. The High Order Y bits must be received first. The $\overline{\text{HIY}}$ signal decoded from the two most significant code bits loads the remaining five data bits into the five Most Significant Bit (MSB) portion of the Y Data Latch. In like manner, the Low Order Y and High Order X bits are loaded into their respective latches. When the fourth byte (Low Order X) is received from the computer, $\overline{\text{LOXE}}$ parallel loads all 20 bits into the X and Y Register. Notice that no storage is needed for the Low Order X inputs because they are the last bits received.

X Register. The X Register is a ten-bit, up-down counter. It is serially operated in Alpha Mode by the LEFT and $\overline{\text{RIGHT}}$ signals, and in GIN Mode by the $\overline{\text{RIGHT}}$ signal. Each low-going $\overline{\text{LEFT}}$ or $\overline{\text{RIGHT}}$ signal will decrement or increment the output one count. It can be parallel loaded by the ten parallel inputs that contain the X coordinate address in Graph Mode operation. The 10 output bits provide a count from 0 to 1023, permitting the display to

be positioned to any one of 1024 separate locations (Tekpoints) in the X Axis.

The CR (Carriage Return), $\overline{\text{HOME}}$, or $\overline{\text{PAGE}}$ signal can reset the X Register to zero. $\overline{\text{HOME}}$ goes active when Terminal power is initialized or when the Reset key is pressed. $\overline{\text{PAGE}}$ goes active when the Page key is pressed, or control character sequence ESC FF is received by the Terminal.

Y Register and Top-of-Page Detect. Like the X Register, the Y Register is serially operated (by $\overline{\text{UP}}$ or $\overline{\text{DOWN}}$) or is parallel loaded (by receiving 10 bits of data from the Y Data Latch). This register is also capable of outputting a count of 0 to 1023. In the X Register, all 1024 of the separate Tekpoints are viewable. In the Y Axis, only 780 of the 1024 Tekpoints are viewable. When a $\overline{\text{PAGE}}$ or $\overline{\text{HOME}}$ signal zeroes the Y Register, inverters cause the register zeroing to be accepted as a 1023 count and the beam is positioned off the top of the screen. Since Page and Home reset Alpha Mode, a Top-of-Page Detect circuit becomes active as soon as the $\overline{\text{HOME}}$ or $\overline{\text{PAGE}}$ signal ends to reset the beam to home position at the top-left in the viewing area.

When the Y Register is zeroed by $\overline{\text{PAGE}}$ or $\overline{\text{HOME}}$, the outputs from the inverters go high, positioning the display beam off-screen at a count of 1023. The two most significant bits (MSB and 2nd MSB) from the inverters are sensed by the Top-of-Page Detect circuit. When both go high, the Top-of-Page Detect circuit places the 614 kHz square wave on the $\overline{\text{DOWN}}$ line, and immediately the display beam begins moving in the down direction. When the count from the Y Register has incremented 256 counts, the 2nd MSB goes low, inhibiting the Top-of-Page Detect circuit and removing the 614 kHz signal from the $\overline{\text{DOWN}}$ line. Thus, the count is stopped at 767 (1023 minus 256 = 767). Notice that incrementing the Y Register results in decrementing the position count. This is true because of the inverters on the output lines.

The MARG signal output is actually an eleventh bit of the Y Register. When the Register decrements one point past the Ø Tekpoint position, MARG goes high while the inverter outputs return the beam to the 1023Y Tekpoint position. When the Y Register again decrements through the Ø Tekpoint position (or when reset by Home or Page), MARG returns low. This signal inputs to the Terminal Busy, Multiplexer, Margin Shifter, and Found circuits (part of Crosshair Generator circuits). Its purpose can be found in the descriptions of each of those blocks.

Terminal Busy. When activated, this circuit holds the Terminal in a "busy" condition. $\overline{\text{TBUSY}}$ goes active low when the $\overline{\text{COUNT IN PROG}}$ signal from the Top-of-Page Detect circuit goes low. This action prevents the reception of data when the Register is counting down to the Home position. This circuit also contains a strappable option that works in conjunction with the MARG signal from the Y Counter. The hardware strap on TC-2 can be installed to make $\overline{\text{TBUSY}}$ go active when line-feeding past the last line of type. To clear the condition, the user must send the $\overline{\text{PAGE}}$ or $\overline{\text{HOME}}$ signals by pressing the PAGE or RESET keys (respectively) on the keyboard, or control character sequence ESC FF must be received by the Terminal.

Margin Shifter. For the Margin Shifter circuit to function, the option strap in the Terminal Busy circuit must be installed in the position that does not give an active $\overline{\text{TBUSY}}$ signal when MARG goes high. Margin 1 is set in the following manner. When in the Alpha Mode, both $\overline{\text{GIN}}$ and $\overline{\text{GRAF}}$ will be inactive and an inactive $\overline{\text{GRAPHICS}}$ signal is input to the Margin Shifter circuit. When MARG goes high and a carriage return has zeroed the X Register, MARG and $\overline{\text{GRAPHICS}}$ combine to put a high on the Most Significant Bit (512) input to the X Digital-to-Analog circuit. This enables the X D/A circuit to output a voltage level that corresponds to the center of the Display Screen. Repeated Carriage Returns will not set the 512 bit low as long as the MARG and $\overline{\text{GRAPHICS}}$ signals are high. $\overline{\text{PAGE}}$ or $\overline{\text{HOME}}$ will inhibit Margin 1 by resetting the X and Y Registers to zero.

X and Y Digital-to-Analog (D/A) Circuits. These circuits convert the digital outputs of the Registers into their respective analog values. Both consist of a diode switching network. The D/A circuits cause a voltage change to occur at their outputs, dependent upon the logic state of the Registers. Notice also, that the X and Y Matrix signals (X MAT, Y MAT) from the Character Generator in TC-1 sum with the register outputs in their respective D/A circuits.

X and Y Filters. The outputs of the X and Y D/A circuits are input to their respective filters. When operating in the Alpha or GIN Mode, $\overline{\text{NOLT}}$ (No Linear Interpolation) will be low. This allows the X and Y analog voltages to pass directly through the circuit to minibus pins M and P.

The Filter circuits are put in use when drawing vectors in the Graph Mode. When the Graph Mode is set, $\overline{\text{NOLT}}$ goes high, activating linear filters within the X and Y Filter circuits.

When $\overline{\text{LOXE}}$ simultaneously loads the 20 bits of data into the X and Y Registers, it causes an almost instantaneous change in voltage to occur at the outputs of the X and Y Digital-to-Analog circuits. This sudden change in voltage cannot be sent directly to the Display Amplifiers because the rate of change is non-linear. In other words, the vector drawn might be very fast at the start and very slow at the end; thus, hardly storing at the beginning and storing very bright at the end, or maybe even over-shooting the defined end point. The filter network overcomes these problems. It provides a linear rate of change in the X and Y output voltages to feed the Deflection Amplifier circuitry.

Data Multiplexer. The Data Multiplexer selects data to be placed on the minibus, outputting five bits (one byte) of data at a time. There are 8 different bytes of data that the Multiplexer can place on the minibus. These include the keyboard bits (b1—b5), Terminal status bits, High Order X bits, Low Order X bits, High Order Y bits, Low Order Y bits, Carriage Return bits, and End of Transmission (EOT) bits. The type of byte being placed on the minibus depends on the output of the 0—7 State Counter circuit.

When data is being sent from the keyboard, the 0—7 State Counter is in its "0" state. This causes the multiplexer to place the complement of the 5 least significant bits of the keyboard character onto the minibus lines. Thus, for this type of operation, it acts as a keyboard to minibus interface. Keyboard data cannot be placed onto the minibus lines until the DATA ENABLE signal from the Strobe Logic circuit goes high. This happens when KSTROBE goes high. (More will be explained about KSTROBE in the description of the Data Logic circuit.) The other types of data bytes are used in the Graphic Input Mode, and will be covered in the descriptions of circuits to follow.

$\overline{\text{BIT 6}}$, $\overline{\text{BIT 7}}$, and $\overline{\text{BIT 8}}$ are placed on the minibus through a special gating network labeled BITS 6, 7, and 8 Gating. When data is being sent from the keyboard, the Step Counter is in State 0. This state allows the Gating circuit to place the complements of keyboard bits 6, 7, and 8 on the minibus when the DATA ENABLE signal goes high, as explained for $\overline{\text{BIT 1}}$—$\overline{\text{BIT 5}}$. (BIT 8 is always high or low as wired at the keyboard.)

Strobe Logic. This circuit mainly controls the various strobe signals associated with Terminal and/or computer operation. KSTROBE goes active high when data is entered from the keyboard. In response to KSTROBE, $\overline{\text{CSTROBE}}$ is generated when $\overline{\text{LOCAL}}$ is high; $\overline{\text{TSTROBE}}$ is generated when $\overline{\text{LOCAL}}$ and $\overline{\text{ECHO}}$ are low; both $\overline{\text{CSTROBE}}$ and $\overline{\text{TSTROBE}}$ are generated when $\overline{\text{LOCAL}}$ is high and $\overline{\text{ECHO}}$ is low. $\overline{\text{ECHO}}$ can be pulled low by a hardwire strap on the Interface card. $\overline{\text{LOCAL}}$ originates from the Local/Line switch on the keyboard. $\overline{\text{CSTROBE}}$ causes data to be sent to the computer; $\overline{\text{TSTROBE}}$ causes data to be executed by the Terminal. Each time $\overline{\text{TSTROBE}}$ or $\overline{\text{CSTROBE}}$ is generated, the DATA ENABLE signal goes high to allow the Data Multiplexer and $\overline{\text{BIT 6}}$, $\overline{\text{BIT 7}}$, and $\overline{\text{BIT 8}}$ Logic outputs to be placed on the minibus.

$\overline{\text{KLOCK}}$ is normally held high on the minibus. Should the user ever have need to inhibit the keyboard, pulling $\overline{\text{KLOCK}}$ low will prevent KSTROBE from affecting the Strobe Logic circuit, thus providing a keyboard lock.

$\overline{\text{CPUNT}}$ is asserted by the Interface Card to prepare the Terminal for data reception from the computer. $\overline{\text{DRBUSY}}$ is asserted by the Hard Copy Unit during copy making or by the Terminal during erase cycles, inhibiting the Strobe Logic circuitry until the operation is complete.

BITS 6, 7, and 8. When sending data from the keyboard, this circuit places the complements of keyboard bits b6, b7, and b8 onto their respective minibus lines. When operating in the Graphic Input Mode, coding signals from the State Decoder set $\overline{\text{BIT 6}}$ high and $\overline{\text{BIT 7}}$ low; $\overline{\text{BIT 8}}$ is arbitrary, being dependent upon the wiring connection of the Terminal keyboard.

Z Control. This circuit is used only in Graph Mode while drawing vectors. It is then enabled by a high $\overline{\text{NOLI}}$ signal. When $\overline{\text{LOXE}}$ initiates a vector, the circuit becomes armed and a 10 μs delay is initiated. If the vector being drawn is less than approximately one-half inch, the three clock pulses (307 kHz, 153 kHz, and 77 kHz) combine to hold $\overline{\text{CGZSUP}}$ low for 11.4 μs out of every 13 μs. The 1.6 μs pulses generated while $\overline{\text{CGZSUP}}$ is high cause dots to be written on the screen. These dots are close enough together to appear as a continuous line. If the vector being drawn is more than approximately one-half inch long, the X D/A or Y D/A signal is large enough to reset the circuit before the 10 μs delay elapses, preventing $\overline{\text{CGZSUP}}$ from going low. The beam is then permitted to be left on during vector drawing.

Crosshair Generator. The Crosshair Generator contains the circuitry needed to generate the crosshair cursor. Its purpose is to determine the digital equivalent of the voltages selected by the X & Y Position Pots, and set the X and Y Registers to that value. The crosshair cursor is generated by alternately incrementing the X Register and decrementing the Y Register. This alternately sweeps the display beam left-to-right and top-to-bottom on the CRT.

The Crosshair Generator is activated when $\overline{\text{CURSE}}$ goes active. $\overline{\text{CURSE}}$ inputs to the Found circuit and sets $\overline{\text{FOUND}}$ high and FOUND low. $\overline{\text{FOUND}}$ enables the Clock circuit which begins sending CLOCK pulses to the Axis Switching and Switch Control circuits. The FOUND signal

going low causes the Strobe Logic circuit to output a low active $\overline{\text{GIN}}$ signal which inputs to U67B, thus inhibiting the Top-of-Page Detect and Margin Shifter circuits. $\overline{\text{CURSE}}$ also presets the Axis Switching circuit to output a low-going $\overline{\text{DOWN}}$ pulse each time the Q output of the Clock circuit pulses high. Each time the $\overline{\text{DOWN}}$ line pulses low, the Y position decrements, causing the display beam to move down one Tekpoint. With each beam movement, the 75 kHz STEP pulse causes an active $\overline{\text{Z}}$ signal to write (but not store) the point.

As the Y Register decrements and moves the display beam downward, the output from the Y D/A circuit changes accordingly and is monitored by the Y Comparator circuit in the Crosshair Generator. When the Y Register has decremented to the point where the voltage from the Y D/A equals, or slightly passes, the voltage from the Y Position Pot, the Y Comparator sends a low $\overline{\text{Y COIN}}$ (Y coincidence) signal to the Memory Gates. While the $\overline{\text{DOWN}}$ line is pulsing, the DOWN signal from the Axis Switching circuit to the Memory Gates is high. When $\overline{\text{Y COIN}}$ goes low, the Memory Gates output a low $\overline{\text{SET}}$ signal to the Switch Control circuit. FOR TC-2 BOARDS WITH NUMBERS 670-1729-04 AND LOWER, THE FOLLOWING OCCURS: The next $\overline{\text{Q}}$ CLOCK pulse clocks the low $\overline{\text{SET}}$ signal into the Switch Control circuit, causing the $\overline{\text{STEP INH}}$ signal to U67D to go low. This inhibits further STEP pulses that were activating $\overline{\text{DOWN}}$ and $\overline{\text{Z}}$ signals. On the next positive going Q CLOCK pulse, the $\overline{\text{SWITCH}}$ signal goes high. When the positive portion of the Q CLOCK pulse ends, the $\overline{\text{SWITCH}}$ signal goes low, putting a low on the DOWN line and a high on the RIGHT line. FOR TC-2 BOARDS WITH NUMBERS 670-1729-05 AND UP, THE FOLLOWING OCCURS: When $\overline{\text{Y COIN}}$ goes low, the Memory Gates output a low $\overline{\text{SET}}$ signal to the Switch Control circuit. The next $\overline{\text{STEP}}$ pulse clocks the low set signal into the Switch Control Circuit, which enables the $\overline{\text{INHIBIT}}$ signal. $\overline{\text{INHIBIT}}$ prevents further $\overline{\text{STEP}}$ signals from activating $\overline{\text{DOWN}}$ and $\overline{\text{Z}}$ signals. On the next positive-going STEP pulse, the $\overline{\text{SWITCH}}$ signal goes high. When the positive portion of the STEP signal ends, the $\overline{\text{SWITCH}}$ signal goes low, putting a low on the DOWN line and a high on the RIGHT line. THIS ENDS DIFFERENCES IN CIRCUIT OPERATION FOR THIS PARAGRAPH.

FOR TC-2 BOARD NUMBERS 670-1729-04 AND LOWER: The end of the high Q CLOCK pulse also causes the $\overline{\text{STEP INH}}$ signal to U67D to go high. Once again, U67D outputs $\overline{\text{STEP}}$ pulses to the Axis Switching circuit. This time the $\overline{\text{RIGHT}}$ line is being pulsed because of the high on the RIGHT line.

FOR TC-2 BOARD NUMBERS 670-1729-05 AND UP: The end of the high STEP pulse also causes the $\overline{\text{INHIBIT}}$ signal to U309A and Axis Switching circuit to go high. Once again U309A begins outputting active $\overline{\text{Z}}$ signals. Also, with $\overline{\text{INHIBIT}}$ high, the $\overline{\text{RIGHT}}$ line can be pulsed because of the high on the RIGHT line.

FOR TC-2 BOARD NUMBERS 670-1729-04 AND LOWER: With U67D enabled, the clock circuit sends out pulses through U67D to generate $\overline{\text{Z}}$ and $\overline{\text{RIGHT}}$ signals until the X Register reaches or slightly passes the value selected by the X Position Pot. When this happens, the output of the X Comparator goes low. The Memory Gates output another low $\overline{\text{SET}}$ signal to the Switch Control circuit. This low permits the Crosshair Generator circuitry to switch from X to Y in a manner similar to that described for Y to X switching.

FOR TC-2 BOARD NUMBERS 670-1729-05 AND UP: With U309A enabled, STEP pulses the $\overline{\text{Z}}$ line until the X Register reaches or slightly passes the value selected by the X Position Pot.

Foldover. Each time the X Register counts through 1023 to 0, the display beam repositions to the left side of the screen and $\overline{\text{SET}}$ returns high. The Register can reset much faster than the display beam can be positioned to the left. Therefore, the counting sequence is interrupted for a short period of time to allow the beam to position to the left and stabilize. When the X Register reaches a count of 1023 the Margin Shifter circuit outputs a low $\overline{\text{EOL}}$ (End of Line) signal. This signal is felt by the Fold Pause circuit in the Crosshair Generator. $\overline{\text{EOL}}$ triggers a one-shot multivibrator within the Fold Pause circuit, causing $\overline{\text{FPAUSE}}$ to go low for 0.5 ms. $\overline{\text{FPAUSE}}$ then inhibits the output of the Clock circuit, preventing further $\overline{\text{RIGHT}}$ pulses. When $\overline{\text{FPAUSE}}$ ends, the X Register continues to increment.

$\overline{\text{SET}}$ also returns high during Y foldover. However, no pause is needed, because the display beam is positioned off-screen when the Y Register resets from 0 to 1023. By the time the Y Register increments enough to bring the display beam into view, it has had adequate time to stabilize.

The above operation of the Crosshair Generator continues until the mode is changed or until the 0 to 7 State Counter is incremented.

Multiplexer Control and Digitization. The Crosshair Generator reflects the digital equivalent of the X and Y Position Pots at the outputs of the X and Y Registers. The process of obtaining the digital equivalent of the Position Pot voltages and sending this to the computer in digital form is known as "digitization". Digitization occurs in a set sequence that is controlled by the Multiplexer Control circuit.

To begin with, assume that the crosshair cursor is running as explained in the preceding description. The $\overline{\text{CURSE}}$ signal, which started the crosshair, also placed a low on the FOUND line to the 0 to 7 State Counter circuit, permitting it to advance on the trailing edge of $\overline{\text{CBUSY}}$ signals. The 0 to 7 State Counter output is at State 0. When it is decided to send the point at which the crosshairs intersect, the user strikes a keyboard key. This causes the keyboard bits to be placed on the minibus by the Multiplexer and sent to the computer (see Table 6-13). When the computer has finished receiving the keyboard data, $\overline{\text{CBUSY}}$ goes high. The next two negative-going transitions of the 614 kHz line advance the State Counter to State 1 and send a PREP pulse to the STROBE Logic circuit. The State Decoder circuit then outputs a low on the STATE line, feeding it back to hold the State Counter enabled.

TABLE 6-13

Data Multiplexer Output Control
(Pertains to each multiplexer device U7, U9, U10, U11, U12)

0–7 State Counter Status	Byte Being Transmitted	Multiplexer Input Control Line Status C (Pin 11)	B (Pin 10)	A (Pin 9)	Multiplexer Y Output (Pin J) Controlled by
0	Keyboard Character	0	0	0	DO (Pin 1)
1	Terminal Status	0	0	1	D1 (Pin 3)
2	High X Bits	0	1	0	D2 (Pin 2)
3	Low X Bits	0	1	1	D3 (Pin 1)
4	High Y Bits	1	0	0	D4 (Pin 15)
5	Low Y Bits	1	0	1	D5 (Pin 14)
6	CR	1	1	0	D6 (Pin 13)
7	EOT	1	1	1	D7 (Pin 12)

The end of the PREP pulse causes the Strobe Logic to output a low $\overline{\text{GO DIGITIZE}}$ signal to the Found circuit. The next time the Crosshair Generator reaches coincidence, the Switch Control circuit sends a $\overline{\text{PT FOUND}}$ pulse to the Found circuit. This causes $\overline{\text{FOUND}}$ to go low, inhibiting the output of the Clock and stopping the count at the Coincidence Point. The outputs of the X and Y Registers then reflect the digital equivalent of the voltage selected by the Position Pots. The low-going $\overline{\text{PT FOUND}}$ signal also causes STATE 2 ADVANCE to go low, advancing the State Counter to State 2. FOUND goes high at the same time, causing the Strobe Logic circuit to become enabled.

With the PREP signal and the FOUND signals high, CSTROBE and DATA ENABLE from the Strobe Logic circuit will activate. With DATA ENABLE high and State 3 selected, the Multiplexer samples the 5 Most Significant Bits of the X Register (High Order X) and sends them along with $\overline{\text{BIT 6}}$, $\overline{\text{BIT 7}}$, and $\overline{\text{BIT 8}}$ to the computer. When the bits are received by the computer, $\overline{\text{CBUSY}}$ once again goes high, advancing the State Counter to State 3 and again initiating CSTROBE and DATA ENABLE action. In turn, the Low Order X, High Order Y, and Low Order Y bits are sent to the computer. The State Counter has now advanced to State 5. At this point, if CR or EOT have not been selected for transmission (by option straps), a COUNTER RESET signal is sent to the 0 to 7 State Counter to return it to 0 and the action ends. If CR has been selected for transmission, the Counter advances to State 6 after the Low Order Y bits are accepted by the computer and $\overline{\text{CBUSY}}$ goes high. CR is strobed to the computer. Again, if EOT has not been selected for transmission, COUNTER RESET ends the action by setting the Counter to 0; otherwise, EOT is sent just as CR was, and the Counter advanced to 0 to end the cycle.

The computer can request the coordinates of the crosshair cursor independent of the user. First it must send ESC plus SUB, causing $\overline{\text{CURSE}}$ to go low to initiate the Crosshair Generator. The computer can then send ESC plus ENQ, causing $\overline{\text{INQUIRE}}$ to pulse low, and the circuitry responds just as though $\overline{\text{CBUSY}}$ had been received after a keyboard character was sent, as previously described. However, a 20 millisecond delay must occur between ESC SUB and ESC ENQ in order for valid X Coordinate data to be generated.

The computer can also request another form of Graphic Input data, independent of the user. This is known as Terminal Status information. If the Terminal is in either Alpha or Graph Mode and the computer sends ESC ENQ, $\overline{\text{INQUIRE}}$ goes low. Since the Counter is at 0 and the crosshair cursor is not running, this causes the State Counter to advance to State 1. The Terminal Status bits MARG, $\overline{\text{GRAF}}$, $\overline{\text{NOLI}}$, $\overline{\text{HCU}}$, and $\overline{\text{AUXSENSE}}$ are sent to the computer as the first byte of the transmission. This is followed by the contents of the X and Y Register and CR and EOT in a manner similar to that previously described. The principal difference is that since the crosshair was not running, no digitization is required and the Multiplexer simply sends the current address of the Alpha cursor or of the Graph beam.

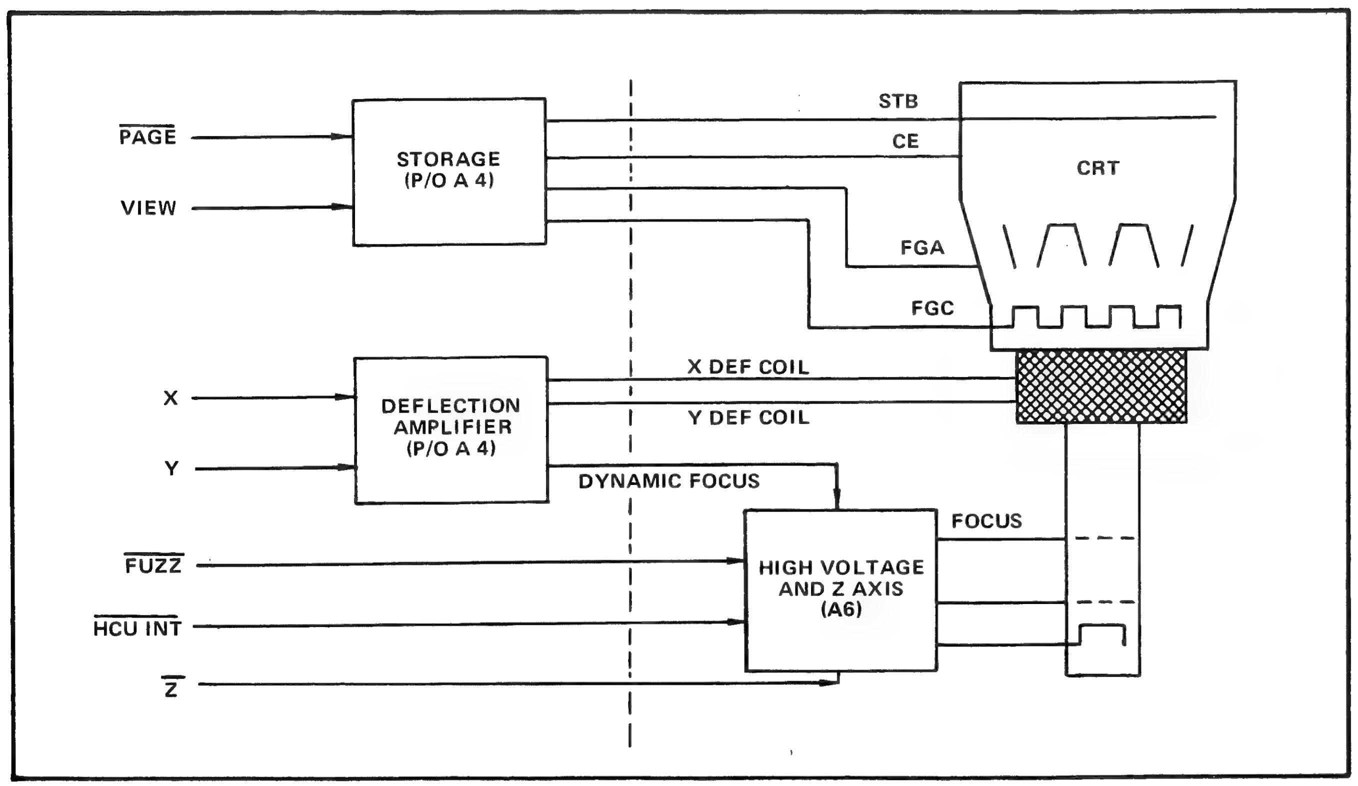


Fig. 6-21. Display Unit Block Diagram.

Ⓐ

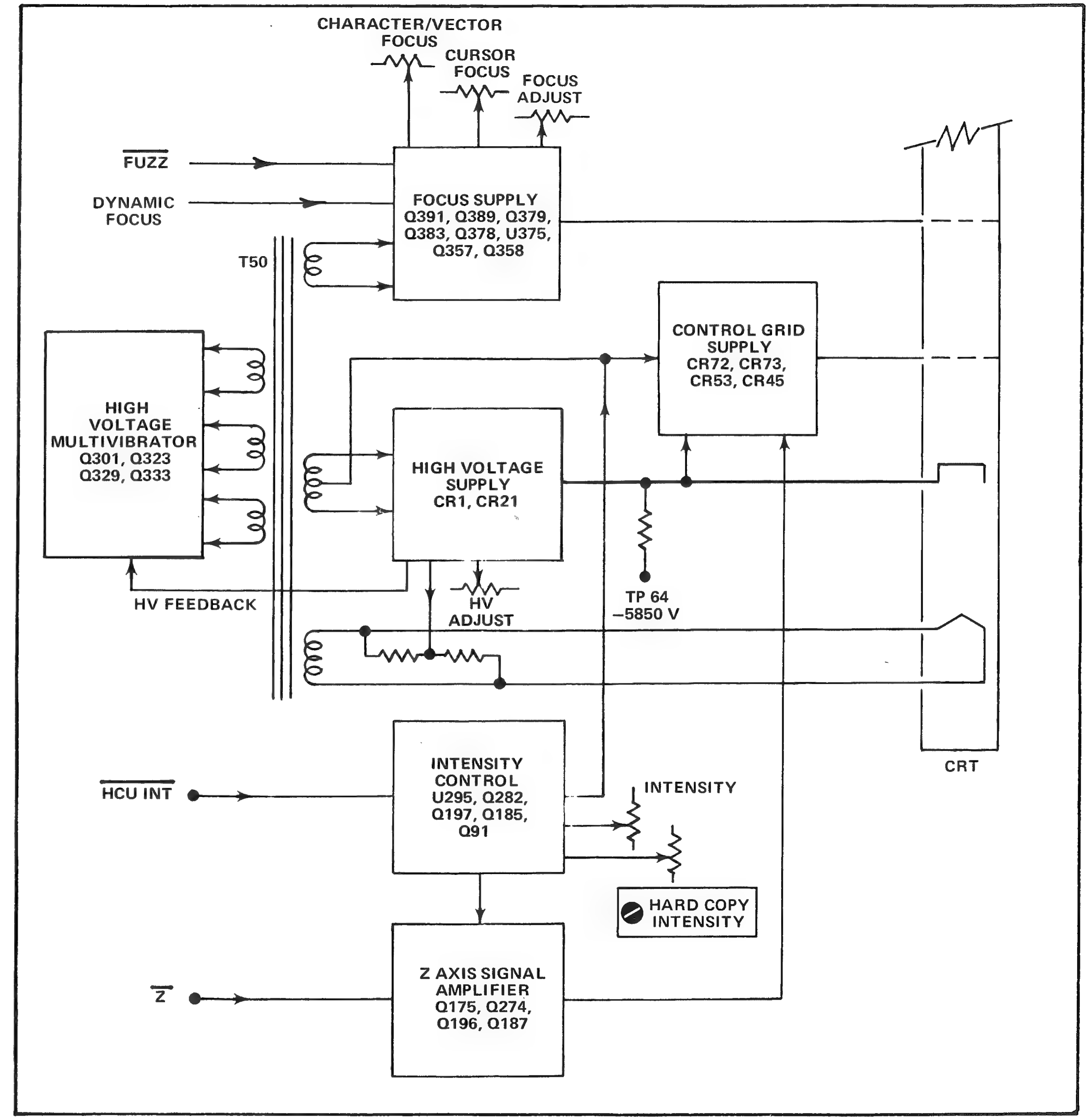
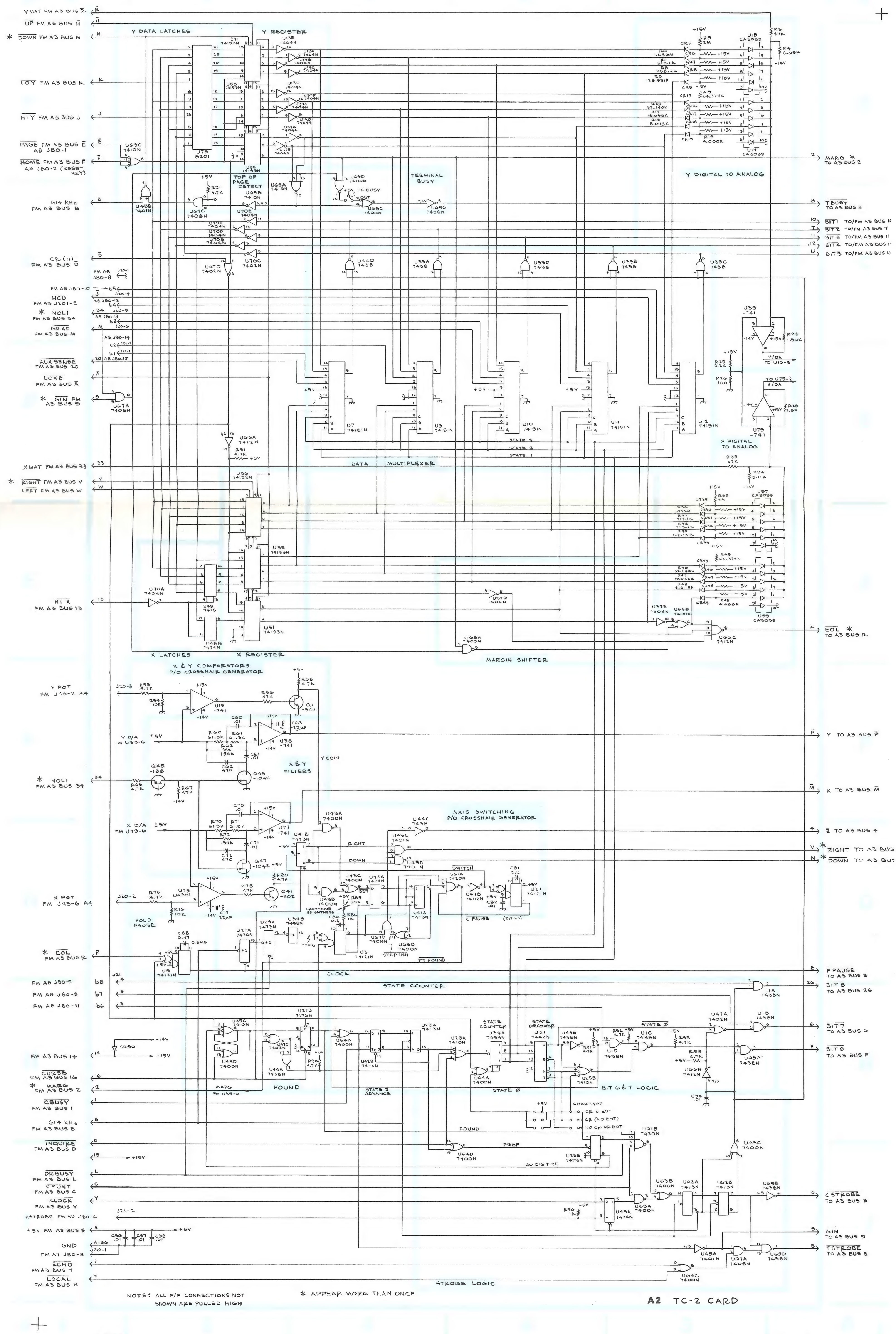


Fig. 6-22. High Voltage & Z Axis Block Diagram.

Ⓐ



A2 TC-2 CARD

4012

FIG 6-20 TC-2

CAPS

CKT NO	GRID LOC
C60	F2
C61	F2
C62	F2
C63	F2
C70	F2
C71	G2
C72	G2
C77	G2
C81	G4
C82	G4
C86	G3
C88	G2
C94	H5
C96	I1
C97	I2
C98	I2

DIODES

CKT NO	GRID LOC
CR5	B5
CR6	B5
CR7	B5
CR8	B5
CR9	B5
CR15	B5
CR16	B5
CR17	B5
CR18	B5
CR19	B5
CR35	E5
CR36	E5
CR37	E5
CR38	E5
CR39	E5
CR45	E5
CR46	E5
CR47	E5
CR48	E5
CR49	E5
CR90	H1

TRANSISTORS

CKT NO	GRID LOC
Q1	F3
Q41	G2
Q43	F2
Q45	F2
Q47	G2

RESISTORS

CKT NO	GRID LOC
R3	B6
R4	B6
R5	B5
R6	B5
R7	B5
R8	B5
R9	B5
R15	B5
R16	B5

RESISTORS

CKT NO	GRID LOC
R17	B5
R18	B5
R19	B5
R21	C2
R23	C6
R25	D5
R26	D5
R28	D6
R33	D5
R34	D5
R35	D5
R36	E5
R37	E5
R38	E5
R39	E5
R45	E5
R46	E5
R47	E5
R48	E5
R49	E5
R51	D2
R53	F2
R54	F2
R56	F2
R58	F3
R60	F2
R61	F2
R62	F2
R65	F2
R67	F2
R70	G2
R71	G2
R72	G2
R75	G2
R76	G2
R78	G2
R80	G2
R85	G3
R86	G3
R90	H3
R91	H4
R92	H5
R93	H5
R96	I4
R98	H5

IC's

CKT NO	GRID LOC
U1A	H5
U1B	H5
U1C	H5
U1D	H5
U3	G3
U5	G2
U7	D3
U9	D3
U10	D4
U11	D4
U12	D5
U13A	B3
U13B	B3
U13C	B3

IC'S

CKT NO	GRID LOC
U13D	B3
U13E	B2
U13F	B2
U15	B5
U17	B5
U19	F2
U21	G4
U23A	H3
U23B	I4
U25A	H4
U25B	H4
U25C	H2
U27A	G2
U27B	H3
U29A	G2
U31	H4
U33A	C3
U33B	C5
U33C	C5
U33D	C4
U34B	G3
U35	B2
U36	E2
U37A	B3
U37B	B2
U37C	B3
U37D	E4
U37E	E5
U37F	B3
U38	F2
U39	C5
U41A	G3
U41B	G3
U42A	G3
U42B	H3
U43A	G3
U43B	G3
U43C	G3
U43D	H2
U44A	H2
U44B	H4
U44C	G3
U44D	C3
U45A	I5
U45B	C2
U45C	G3
U45D	G3
U47A	H5
U47B	G4
U47C	H2
U47D	C2
U48B	E2
U49	E2
U51	E2
U53	B2
U55	E2
U57	E5
U59	E5
U61A	G4
U62A	I5
U62B	I5

IC'S

CKT NO	GRID LOC
U63A	I5
U63B	I5
U63C	I5
U63D	G3
U64A	H4
U64B	H3
U64C	I5
U64D	I4
U65A	H5
U65B	I6
U65C	C3
U65D	I6
U66A	D2
U66B	H5
U66C	E5
U67A	I5
U67B	D1
U67C	C2
U67D	G3
U68A	E4
U68B	E5
U68C	C3
U68D	C3
U69A	C3
U69B	C2
U69C	B2
U70A	E2
U70B	C2
U70C	C2
U70D	C2
U70E	C2
U70F	C2
U71	B2
U73	B2
U75	G2
U77	G2
U79	D5

A

TC-2 Semiconductor Information

NUMBER	VCC	GND	UNUSED INPUTS
7400	14	7	HIGH
7401	14	7	HIGH
7402	14	7	LOW
7404	14	7	
7408	14	7	LOW
7410	14	7	HIGH
7412	14	7	HIGH
7420	14	7	HIGH
7438	14	7	HIGH
7442	16	8	
7473	4	11	HIGH
7474	14	7	HIGH
7475	5	12	HIGH
7476	5	13	HIGH
7493	5	10	LOW
74121	14	7	HIGH
74151	16	8	
74193	16	8	LOW

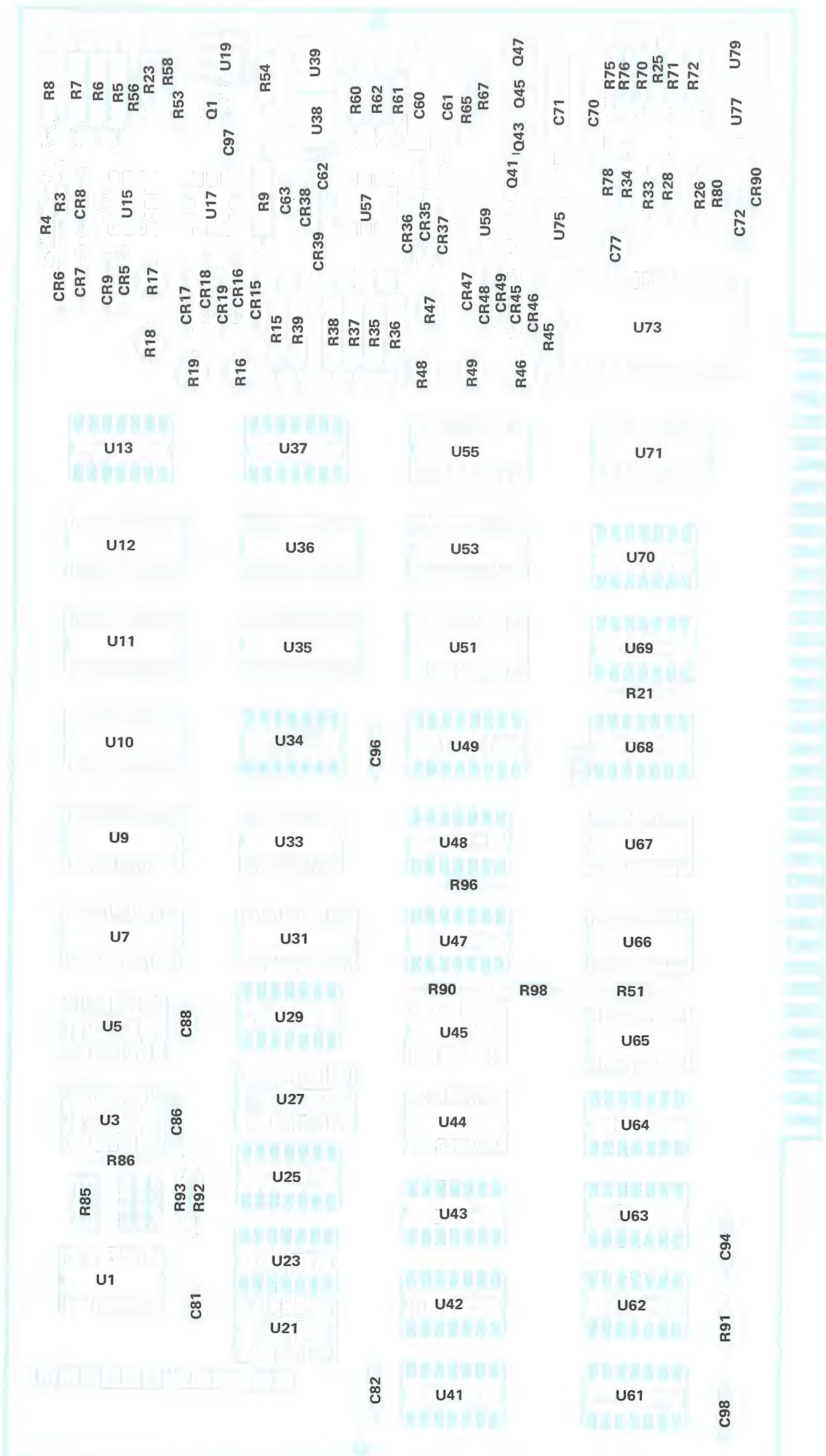


Fig. 6-19. TC-2 Component Locations.

Ⓐ

DISPLAY UNIT

Display Unit Block Diagram Description

A block diagram of the Display Unit (exclusive of keyboard and Hard Copy consideration) is shown in Fig. 6-21. The writing portion of the Display Unit consists of a High Voltage and Z Axis circuit, a Deflection Amplifier circuit, X and Y Deflection Coils, and the writing components of the CRT — namely the Cathode, Control Grid, and Focus Anode. The storage section consists of the Storage circuitry and the storage components of the CRT — the Flood Gun Cathode (FGC), the Collimation Electrode (CE), the Flood Gun Anode (FGA), and the Storage Backplate (STB). The writing portion of the Display Unit controls beam positioning and writing, while the storage portion controls and maintains the intensity of stored information.

Positioning information is received in the form of X and Y analog signals into the Deflection Amplifiers. These generate a positioning current in the X deflection coil and Y deflection coil, and also causes a DYNAMIC FOCUS signal to be sent to the High Voltage and Z Axis circuit. This DYNAMIC FOCUS signal is minimum for center screen position, and maximum for edge position. (Dynamic Focus is necessary because focusing is partially dependent on beam travel distance, and the beam must travel further in reaching the edges of the CRT than it does in reaching the center of the CRT.) The $\overline{\text{FUZZ}}$ signal is LOW during Alpha cursor generation and GIN Mode to provide optimum focusing for those refreshed displays. During Alpha character writing time, and in Graph Mode, $\overline{\text{FUZZ}}$ goes high to permit separate focusing for stored writing. The $\overline{\text{Z}}$ signals into the High Voltage and Z Axis circuit control the Grid Bias. The $\overline{\text{HCU INT}}$ signal modifies the CRT intensity to accommodate hard copy operation. Additional information regarding hard copy writing is available elsewhere in this section.

The storage circuitry responds to two input signals and provides the cathode-ray tube with four operating voltages. Assuming that $\overline{\text{PAGE}}$ and VIEW are both high, the Flood Gun Cathode continuously emits electrons that are accelerated by the Flood Gun Anode. These strike the Storage Backplate, where they continuously reinforce the stored information. If no inputs are received by the Terminal for approximately 90 seconds, the VIEW signal goes low, causing the Flood Gun Anode voltage to drop to a level below that of the cathode. This reduces the flow of electrons from the Flood Gun Cathode and drops the CRT Intensity below viewing level.

The $\overline{\text{PAGE}}$ signal causes the CRT and Storage circuits to go through an Erase cycle. The four storage signals then cycle through a change in voltages, which causes the CRT to become totally written and then to completely erase.

High-Voltage and Z Axis Circuits

Block Diagram Description. Refer to the block diagram of the High-Voltage circuits, which is shown in Fig. 6-22. These circuits control the filament supply, the cathode supply, the control grid supply, and the focus supply for the writing gun of the CRT. A High Voltage multivibrator drives a transformer to produce the various voltages required by the circuits. The multivibrator receives drive from one of the secondary windings, and also receives biasing voltage for its control amplifier from a secondary winding. In addition, a high voltage feedback signal is applied to the multivibrator to keep the high voltage at a given value. CR1 and CR21 help to provide a −5850 cathode voltage supply, and filament voltage is obtained from a secondary winding of T101. The Control Grid circuit and Filament circuit are both referenced to the −5850 power supply.

A tap from a secondary winding (which powers the high-voltage supply) sends additional voltage to the control-grid supply to enable it to provide a control-grid voltage which is more negative than the cathode voltage. The actual difference between the two is a function of the Intensity Control circuit and the Z Axis Signal Amplifier. If the $\overline{\text{HCU INT}}$ and $\overline{\text{Z}}$ signals are high, this difference is approximately 100 volts. When $\overline{\text{HCU INT}}$ is low, this difference increases to approximately 115 volts. When $\overline{\text{HCU INT}}$ is high and $\overline{\text{Z}}$ is low, this difference becomes approximately 50 volts, permitting stored writing to occur.

Another secondary winding of T101 provides the Focus Supply circuit with enough drive to develop negative high voltage for the focus anode. Focus Adjust permits optimum overall focusing. A dynamic focus amplifier works in conjunction with the high voltage focus supply. The DYNAMIC FOCUS signal compensates for defocusing due to the writing beam deflection from CRT center to CRT edge. There are two dynamic focus adjustments. Character/Vector Focus provides for uniform focusing throughout the display area during Alpha Mode character Writing and during Graph Mode. Cursor Focus permits optimum focusing during Alpha cursor and Crosshair Cursor Generation when $\overline{\text{FUZZ}}$ is low.

High-Voltage Oscillator. Refer to the High-Voltage and Z Axis schematic diagram, Fig. 6-24. Oscillator Q301 provides current to the primary winding of T101. When current in this winding is increasing, a secondary winding provides positive voltage to the base of Q301. When Q301 collector current reaches Beta times its base drive, Q301 unsaturates and the primary winding voltage decreases. Thus, the positive voltage to the base of Q301 decreases. When the voltage at the base of Q301 becomes sufficiently low, Q301 stops conduction, causing a further decrease in the primary voltage. This causes a negative voltage to be applied to the base of Q301, driving this transistor further into cut-off. When C209 discharges sufficiently, the voltage at the collector of Q323 rises and the cycle repeats itself. The Q301 drive current is obtained by charging capacitor C209. However, part of the C209 charging current is also obtained from Q323. Therefore, changes in Q323 collector current affect the drive to Q301. Q323 current is controlled by a feedback from the high-voltage circuit, adjustable by R227.

High-Voltage Supply. Power for this supply is provided by the 8—13 winding. Voltage from this secondary is doubled by C16, CR1, CR21, and C138. The filtered —5850 volts is then applied to the cathode of the CRT. The unfiltered high voltage is connected through R38 and R40 to the two sides of the filament supply, elevating it to the proximity of the voltage on the CRT.

Control Grid Supply. The —5850 cathode voltage is felt on C65, via CR45, R47, and R55. Assuming that pin 14 of the transformer is at zero volts, C65 charges to 5850 volts. With $\overline{\text{HCU INT}}$ high, the voltage at the wiper of R86 is at approximately 100 volts. During one-half cycle of operation, pin 14 of T101 goes positive; CR74 and CR79 go into conduction and limit the voltage to about 100 volts at the CR74-CR79 junction. This causes C65 to charge an additional 100 volts, ending up with about 5950 volts across it. Assume the $\overline{\text{HCU INT}}$ and $\overline{\text{Z}}$ signals are both high. The voltage at the top of DS74 is then about +5 volts. When pin 14 of T101 swings negative, CR72 conducts and clamps the bias signal from going below +4.5 volts. However, the 95 V decrease on one side of C65 causes the other side to decrease by an equal amount. As the high voltage side of C65 goes negative to —5945 V, CR45 becomes back-biased. CR53 conducts and C64 charges toward —5945 V; the control grid voltage is placed 95 volts below the cathode voltage, blanking the writing beam. The circuit then acts as a peak detector and maintains the blanking bias value until writing is commanded.

Intensity Control Circuit. A regulated +250 V for the Intensity Control circuit is supplied by series regulator Q197. The 250 V at its emitter is sampled by the R195-R193 voltage divider. Any voltage deviation is felt at pin 13 of U295 (a high-gain operation amplifier), which sends a correction voltage to Q282. The resultant change in drive signal to the base of Q197 holds the +250 V supply within design limits.

Q185 and Q91 are supplied by the +250 V from Q197 and from a dual Intensity Control circuit. With $\overline{\text{HC INT}}$ high, Q185 is allowed to conduct, where approximately 100 volts is selected at the wiper of R86. (This is variable between +15 and +215 volts due to CRT bias requirements.) This voltage then controls the CRT grid bias as explained in the Control Grid Supply description.

When a hard copy is commanded, the $\overline{\text{HC INT}}$ line goes low, turning Q185 off and allowing Q91 to conduct. This permits C65 in the Control Grid Supply to charge to a higher value, as set by R91, when a hard copy is requested. With the voltage at the top of DS74 still at +5 volts, C64 is permitted to increase its charge accordingly, increasing the voltage difference between the Control Grid and the cathode of the CRT. This increase in bias is necessary for hard copy operation.

Z Axis Signal Amplifier. The beam writing voltage at the top of DS74 is controlled by the $\overline{\text{Z}}$ signal. When $\overline{\text{Z}}$ is active, the voltage is about 75 volts and writing is permitted. When $\overline{\text{Z}}$ is inactive, the voltage remains at +5 V. When $\overline{\text{Z}}$ is high, Q175 is turned on via bias network R179, R183, R280, R181, and R281. Q175's collector pulls down to about +6 volts. Diode CR178 keeps Q175 from saturating for turn-off speed considerations. This voltage is felt through emitter-follower Q274, and is used as a reference voltage for the Control Grid Supply circuit as previously explained.

When $\overline{\text{Z}}$ goes low to command the beam to write, Q175 cuts off and its collector rises toward 175 volts. However, notice that the biasing voltage of Q196 holds the emitter voltage of Q187 at about 75 volts. This voltage is felt on the cathode of CR177. As long as the anode of CR177 is held below 75 volts, CR177 cannot conduct. This is the case with the $\overline{\text{Z}}$ signal inactive. Now, when the collector of Q175 rises to about 75 V, CR177 goes into conduction and holds the collector of Q175 at that value. Approximately +75 V appears on the emitter of Q274 and replaces the +5 volts previously present at the top of DS74.

The change in voltage at the top of DS74 has an effect on the CRT Control Grid Bias. When the bias signal at the

Ⓐ

CR74-R77 junction drops to approximately 75 volts, CR72 goes into conduction and holds it at that value rather than permitting it to go to +5 V as before. The voltage swing at the CR73-C65 junction is therefore limited to 20 volts. Since the high voltage side of C65 follows suit, the voltage difference between grid and cathode decreases to approximately 20 volts, permitting information to be written on the CRT. L173 (in the Q175 collector circuit) increases the switching action during writing time, by helping overcome the capacitance inherent in the Control Grid circuit.

Focus Circuit. The Focus circuit is designed to provide optimum focusing in all modes of operation. The circuit consists of a floating Focus High-Voltage Power Supply, Alpha and Vector Focusing Adjust circuits, a Constant Current circuit, an Operational Amplifier, and a grounded-base amplifier used as a logic switch.

Operation of the circuit during Alpha Mode with the cursor in a corner of the CRT will be explained first. Under this circumstance, approximately 8 volts of focus correction signal is received at the DYNAMIC FOCUS input. Since this 8 volts is applied to voltage divider R379 and R371, it causes approximately 0 volts at the negative input of amplifier U375. U375 drives Q358 until the Q358 collector voltage is sufficiently positive to drive the positive input of U375 to 0 volts to balance it with the negative input. With the positive input at 0 volts, no current can flow through Q378 or Q389, since their sources are also at 0 volts. Constant Current circuit Q383 causes 0.3 milliampere to enter the circuit through the Q383 collector. The 0.3 mA is the only current flowing through feedback resistor R366, setting the R366-R355 junction (via feedback operation) to 150 volts. Approximately 150 volts is therefore felt at the emitter of Q357, providing a reference voltage for one side of the Focus High Voltage Power Supply. The Focus High Voltage Power Supply generates approximately —5850 volts, just as the Cathode circuit high voltage winding does. A portion of this voltage is picked off by the Focus Adjust potentiometer and applied to the Focus Grid of the CRT.

When generating a character or drawing a vector, $\overline{\text{FUZZ}}$ is high, turning Q389 on and Q378 off. This enables Character/Vector Focus Adjust R389. Note that with Q379 cut off and 0 volts on both sides of R389, neither the Character/Vector Focus or the Cursor Focus has any control; focusing is totally dependent upon the position of R161 for CRT corner focus. When the beam is moved to the center of the CRT, the Dynamic Focus voltage returns to approximately 0 V. The R379-R371 voltage divider applies approximately —5 volts to the negative input of U375. This causes U375 to drive Q358 until its collector is sufficiently low to permit the positive input of U375 to reach the value present on the negative input — approximately —5 volts. With $\overline{\text{FUZZ}}$ high, Q389 acts as a short circuit. With the Character/Vector Focus potentiometer near midrange, R389 and R387 now demand approximately 0.08 mA of current. With 0.3 mA available from Q383, this leaves approximately 0.22 mA available to flow through R366, indicating that the collector of Q358 must be at approximately +105 volts. The focus reference voltage at the emitter of Q357 is therefore approximately +105 volts. Since current now is flowing through R389, the Character/Vector Focus Control is effective, and can be made to set the Q357 voltage to any value between approximately 85 and 115 volts, thereby controlling the focusing of the display near center of the CRT.

When generating an Alpha or crosshair cursor, $\overline{\text{FUZZ}}$ goes low and turns Q389 off and Q378 on. This causes Q378 to act as an effective short circuit, supplying current for the Cursor Focus potentiometer. As with the Character/Vector Focus control, Cursor Focus R382 only has effect on the display when the CRT beam is not located at any of the extreme corners of the CRT.

In summary, the circuit allows R161 (Focus Adjust) to adjust for good corner focus, R389 (Character/Vector Focus) to adjust for best Alpha and Vector Focus ($\overline{\text{FUZZ}}$ high), and R382 (Cursor Focus) to adjust for best center screen focus ($\overline{\text{FUZZ}}$ low).

Miscellaneous Components. Neon lamps appear in various parts of the High Voltage circuit. These lamps are intended primarily as arc protection devices. At any time a radical change occurs in the voltage of any section of the High Voltage circuit, these lamps fire and cause the remainder of the circuitry to stay electrically close together to avoid breakdown between the circuits.

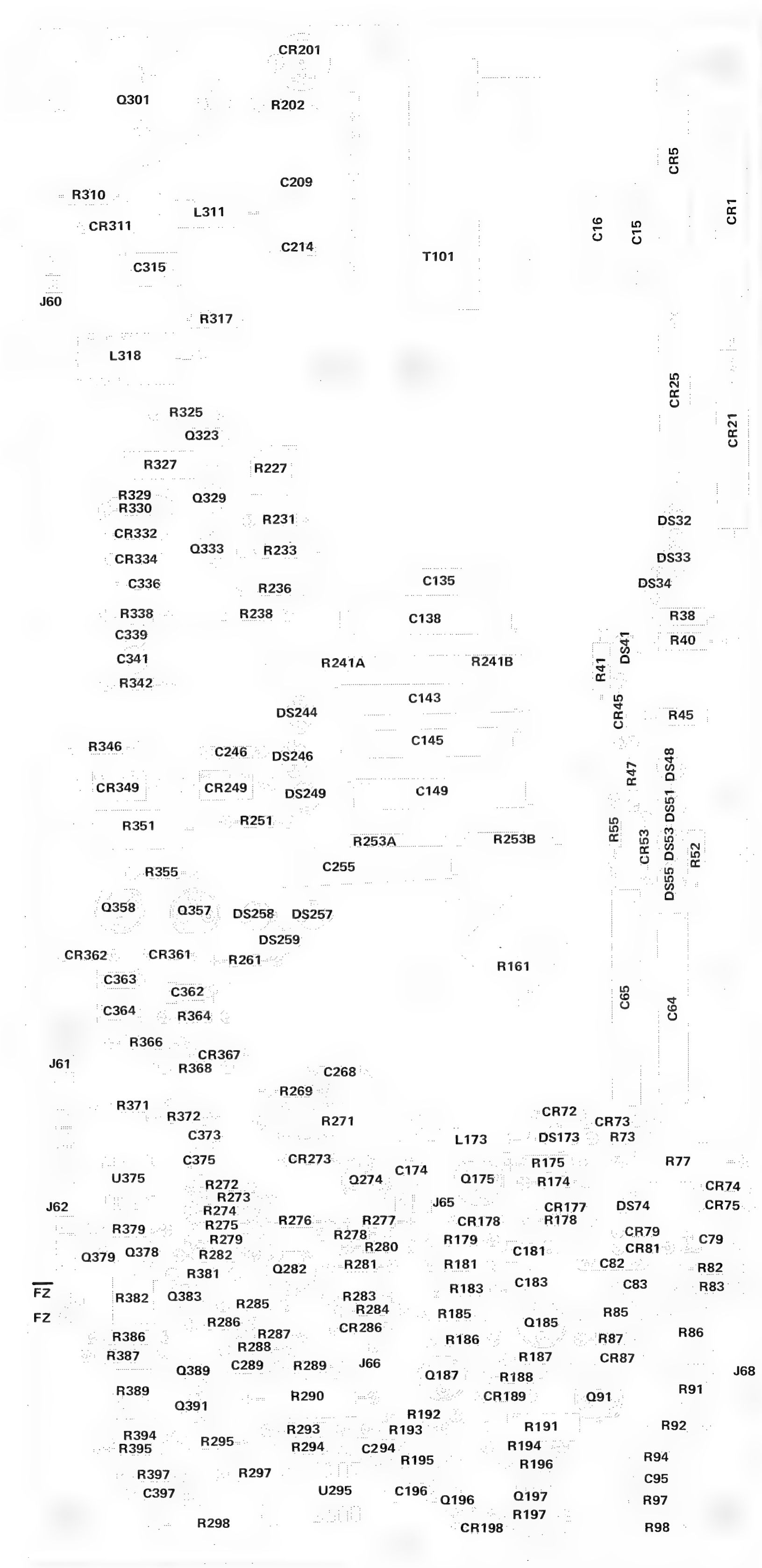


Fig. 6-23. High Voltage and Z Axis Component Locations.

Ⓐ

DEFLECTION AMPLIFIERS
BLOCK DIAGRAM

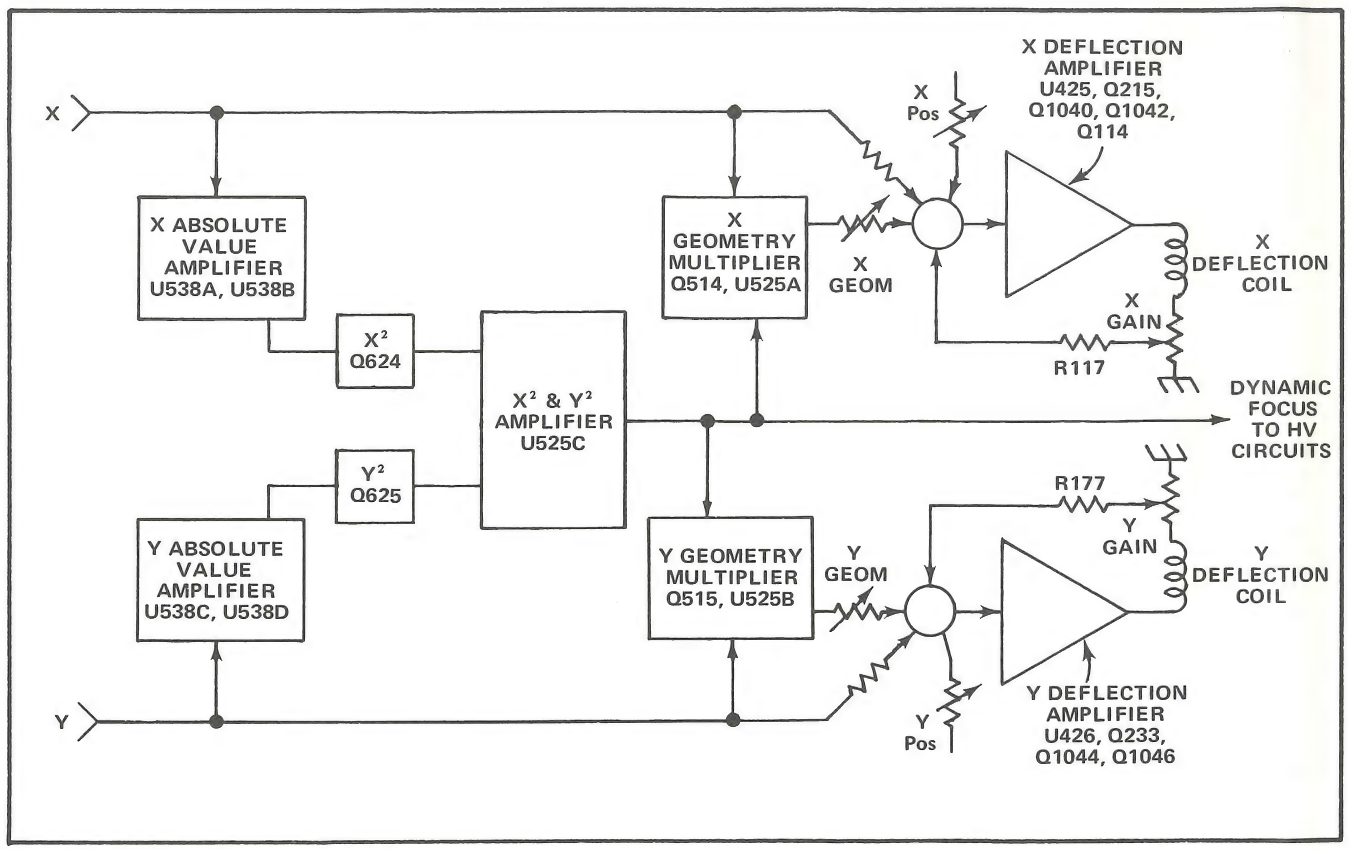


Fig. 6-25. Deflection Amplifier Block Diagram.

Ⓐ

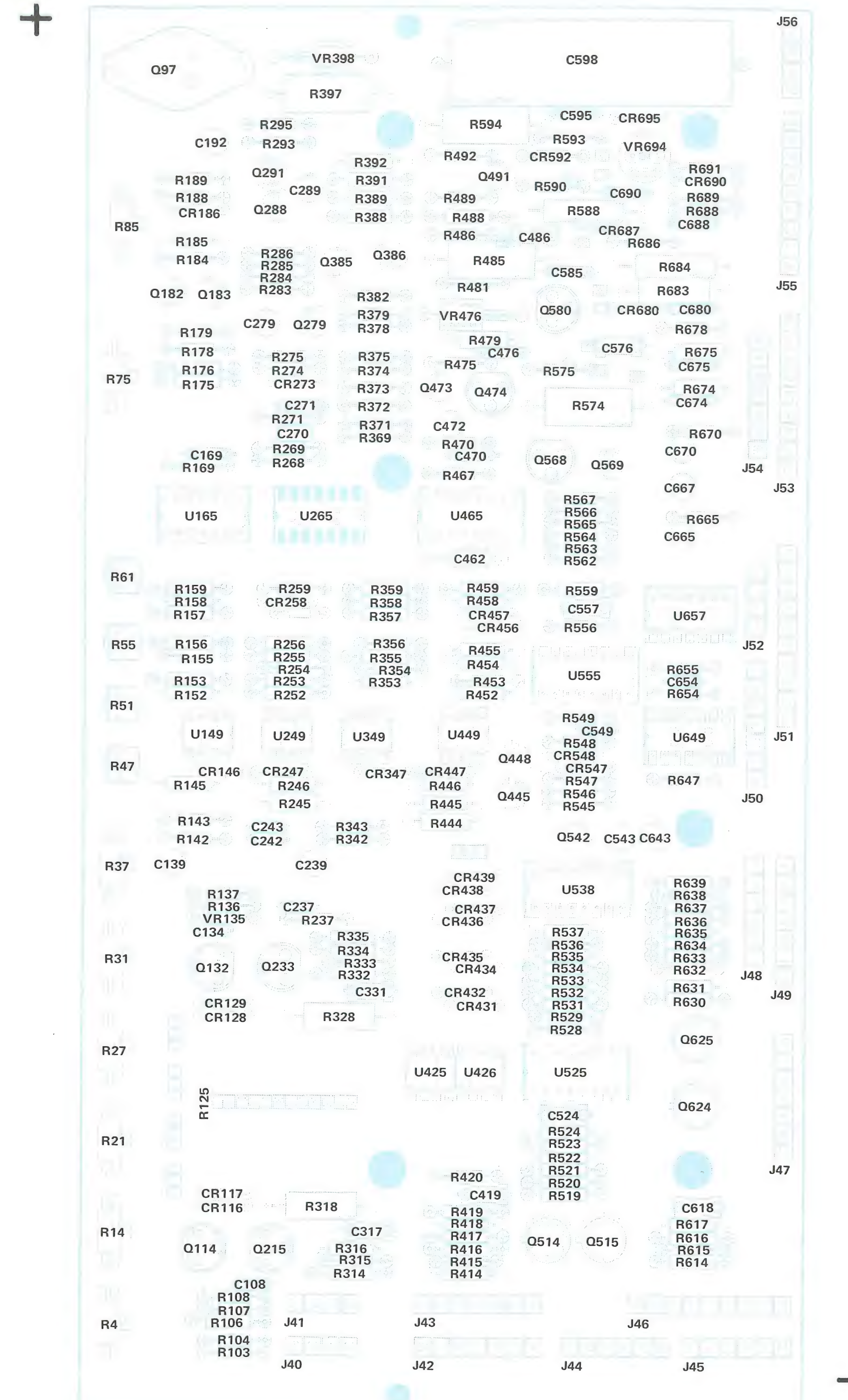


Fig. 6-26. Deflection Amp and Storage Component Locations. Boards #670-2571-00, 01, 02.

Ⓐ

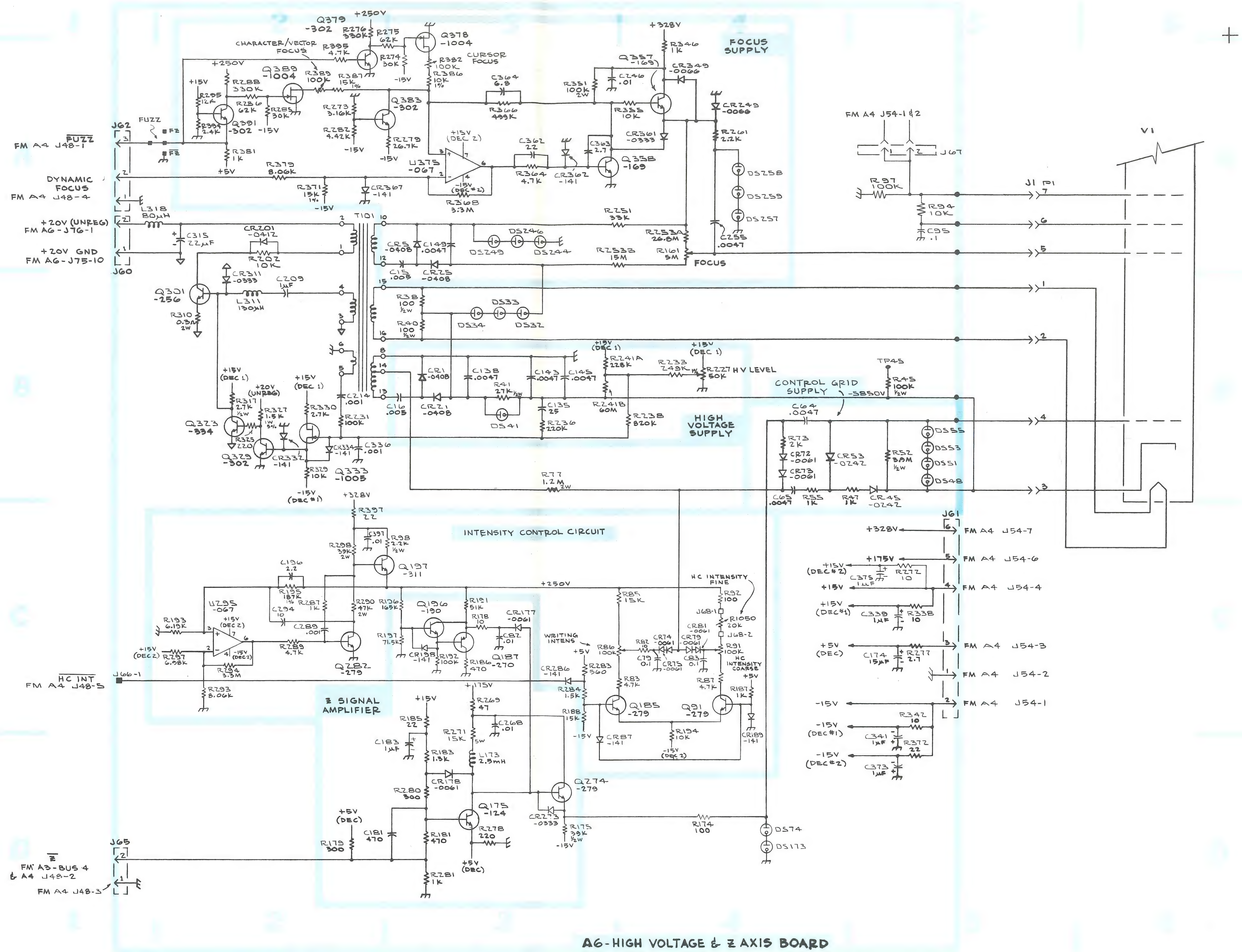


FIG 6-24 HIGH VOLTAGE & Z AXIS

HIGH VOLTAGE & Z AXIS

BULBS

CKT NO	GRID LOC
DS32	B3
DS33	B3
DS34	B3
DS41	B3
DS48	B5
DS51	B5
DS53	B5
DS55	B5
DS74	D4
DS173	D4
DS244	A3
DS246	A3
DS249	A3
DS257	A4
DS258	A4
DS259	A4

CAPS

CKT NO	GRID LOC
C15	A3
C16	B3
C64	B4
C65	B4
C79	C4
C82	C3
C83	C4
C95	A5
C135	B3
C138	B3
C143	B3
C145	B3
C149	A3
C174	C5
C181	D3
C183	D3
C196	C2
C209	B2
C214	B2
C246	A3
C255	A4
C268	C3
C289	C2
C294	C2
C315	A2
C336	B2
C339	C5
C341	D5
C362	A3
C363	A3
C364	A3
C373	D5
C375	C5
C397	C2

DIODES

CKT NO	GRID LOC
CR1	B3
CR5	A3
CR21	B3
CR25	A3
CR45	B5
CR53	B4
CR72	B4
CR73	B4
CR74	C4
CR75	C4
CR79	C4
CR81	C4
CR87	D3
CR177	C3
CR178	D3
CR189	C4
CR198	C3
CR201	A2
CR249	A4
CR273	D3
CR286	C3
CR311	B2
CR332	B2
CR334	B2
CR349	A4
CR361	A4
CR362	A3
CR367	A2

INDUCTORS

CKT NO	GRID LOC
L173	D3
L311	B2
L318	A1
L318	A2

TRANSISTORS

CKT NO	GRID LOC
Q91	C4
Q175	D3
Q185	C3
Q187	C3
Q196	C3
Q197	C2
Q274	D3
Q282	C2
Q301	B2
Q323	B2
Q329	B2
Q333	B2
Q357	A4
Q358	A3
Q378	A3
Q379	A2
Q383	A2
Q389	A2
Q391	A2

RESISTORS

CKT NO	GRID LOC
R38	B3
R40	B3
R41	B3
R45	B5
R47	B5
R52	B5
R55	B4
R73	B4
R77	B3
R82	C4
R83	C4
R85	C4
R86	C4
R87	C4
R91	C4
R92	C4
R94	A5
R97	A5
R98	C2
	C3
R161	A4
R174	D4
R175	D3
R178	C3
R179	D2
R181	D3
R183	D3
R185	C3
R186	C3
R187	C4
R188	C3
R191	C3
R192	C3
R193	C2
R194	D4
R195	C2
R196	C3
R197	C3
R202	A2
R227	B4
R231	B2
R233	B4
R236	B3
R238	B4
R241A	B3
R241B	B3
R251	A4
R253A	A4
R253B	A4
R261	A4
R269	C3
R271	C3
R272	C5
R273	A2
R274	A3
R275	A3
R276	A2
R277	C5
R278	D3
R279	A3
R280	D3
R281	D3
R282	A2
R283	C3
R284	C3
R285	A2
R286	A2
R287	C2
R288	A2

RESISTORS

CKT NO	GRID LOC
R289	C2
R290	C2
R293	C2
R294	C2
R295	A2
R297	C2
R298	C2
R310	B2
R317	B2
R325	B2
R327	B2
R329	B2
R330	B2
R338	C5
R342	C5
R346	A4
R351	A3
R355	A4
R364	A3
R366	A3
R368	A3
R371	A2
R372	D5
R379	A2
R381	A2
R382	A3
R386	A3
R387	A2
R389	A2
R394	A2
R395	A2
R397	C2
R1050	C4

IC's

CKT NO	GRID LOC
U295	C2
U375	A3

TRANSFORMERS

CKT NO	GRID LOC
T101	A2
	B2

Ⓐ

Deflection Amplifiers Description

General. The Deflection Amplifier circuit uses the X and Y analog voltages and amplifies them to provide the drive signals to the X and Y deflection coils. This circuit also generates a dynamic focus signal that is used in the High-Voltage circuit.

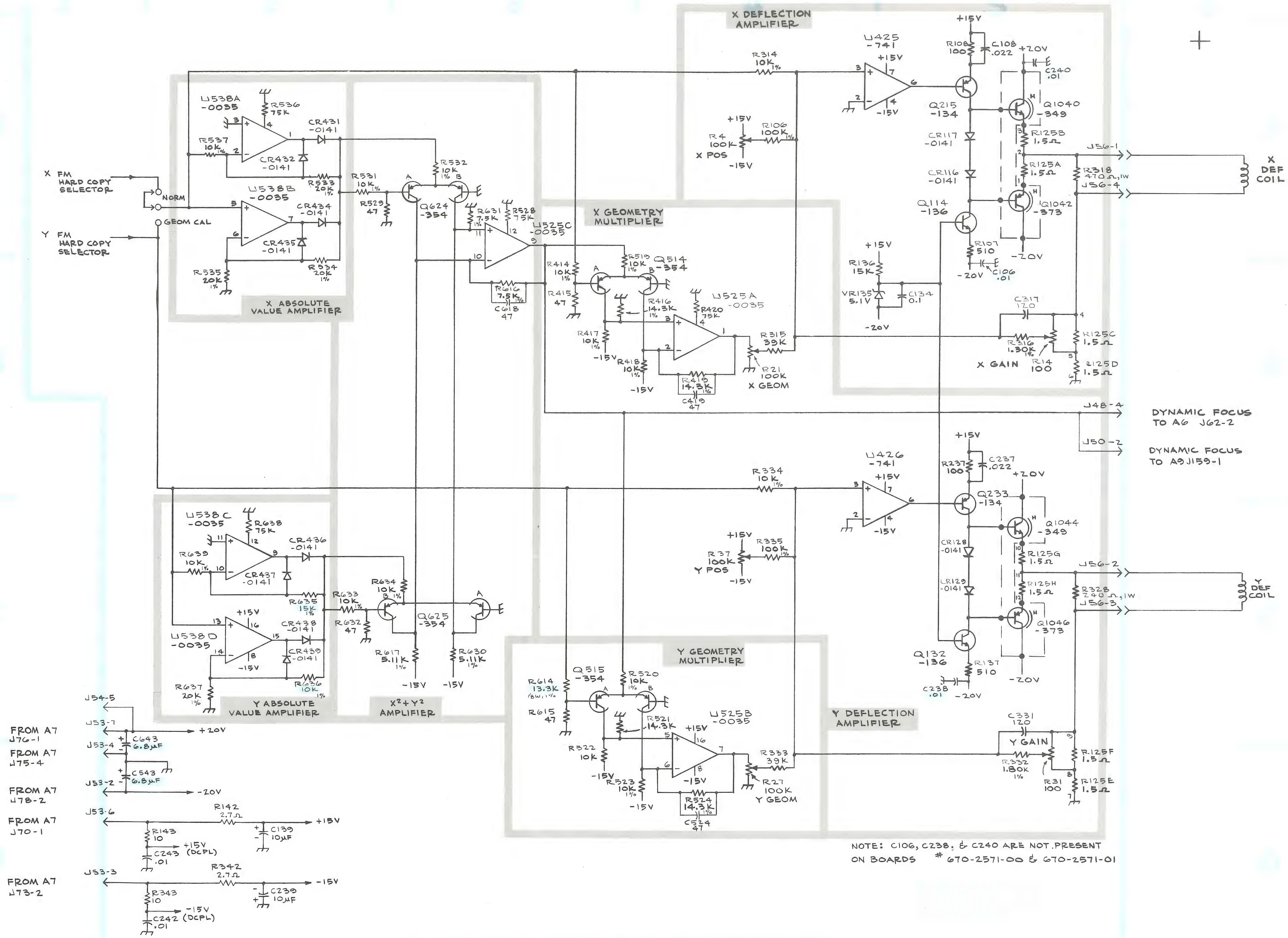
Block Diagram Description. Refer to the block diagram in Fig. 6-25. The circuits making up the deflection amplifiers are the X Absolute Value Amplifier, the Y Absolute Value Amplifier, the X^2 and Y^2 circuits, the $X^2 + Y^2$ Amplifier, the X Geometry Multiplier, the Y Geometry Multiplier, the X Deflection Amplifier, and the Y Deflection Amplifier.

The X and Y signals are each applied to three circuits within the deflection amplifiers. The X signal goes to the X Absolute Value Amplifier to generate a positive output signal regardless of the polarity of the X Input signal. Then it is squared and applied to the $X^2 + Y^2$ Amplifier. It is combined with the positive signal from the Y^2 circuit to develop the Dynamic Focus signal, which goes to the X Geometry Multiplier and the Y Geometry Multiplier, as well as going to the High Voltage circuits. The X input signal is also applied to the X Geometry Multiplier circuit, where it combines with the Dynamic Focus signal to generate an X Geometry signal. The X signal, X Geometry signal, and a Feedback signal from the X Deflection Amplifier combine at the summation point at the input to the X Deflection Amplifier. The output of the X Deflection Amplifier provides the drive for the X Deflection coil. The Y Deflection Amplifier circuit functions in a similar manner.

Detailed Description. Refer to the Deflection Amplifier schematic, Fig. 6-27. Because of the similarity between the X circuitry and the Y circuitry, only the X circuits will be explained here. The X Absolute Value Amplifier consists of two operational amplifiers, each of which has one input referenced to ground. If a negative X signal is applied, U538A develops a positive-going output which back-biases CR432 and forward-biases CR431, permitting the signal to be felt at the emitter and base of Q624. The negative X signal is simultaneously applied to the positive input of U538B, causing its output to go negative. CR434 becomes back-biased, preventing the signal from affecting the output. CR435 becomes forward-biased, permitting feedback to pin 6 to offset the input signal. If the X input goes positive, U538B develops a positive output, forward-biasing CR434 and transmitting the signal to Q624. The positive X applied to U538A causes its output to go negative, back-biasing CR431 and forward biasing CR432, holding pin 2 at ground potential.

X^2 amplifier Q624 is cut off under no-signal conditions. Positive voltages applied to R532 cause the transistor to conduct. However, the same positive voltage being applied to R532 is also applied to the R531-R529 voltage divider. This causes the current through one side of Q532 to be less than the current through the side that has its base grounded. The difference between the output signals taken from the collectors of Q532 is then approximately proportional to the square of the input voltage. The signals combine with the signals from Q625 in the Y^2 Amplifier, with the resultant signal being applied to the inputs of U525B. U525B develops an $X^2 + Y^2$ output, which it applies to the emitter of Q514. Q514 has a portion of the X input signal applied to the base of one-half of the transistor, causing the difference outputs at the collectors of Q514 to be approximately equal to $KX\ (X^2 + Y^2)$. These are applied to amplifier U525A, developing an output signal which is used as geometry correction. A portion of this is picked off by R21, which demands current through R315 from the summation point at pin 3 of U425 via R315. The X input signal also demands current via R314, while the positioning potentiometer R4 demands current through R106. U425 responds by developing an in-phase output signal at pin 6. Q215 amplifies and inverts the output of U425, applying it to complementary emitter-followers Q1040 and Q1042. A portion of the signal from Q1040 and Q1042 is felt at R14, which supplies the current demanded by R315, R314, and R106, while permitting pin 3 of U425 to remain near zero volts as dictated by pin 2 of U425.

Under no-signal conditions, the R318-R125 junction is at zero volts, resulting in no current through the X Deflection Coil. If U425 outputs a negative voltage, Q215 develops a positive voltage at its collector, which is felt through the emitters of Q1040 and Q1042. The R318-R125 junction goes positive, causing electron flow up through the coil. If the pin 6 output of U425 goes positive, Q215 delivers a negative through the base-emitter junctions of Q1040 and Q1042, causing electron flow down through the X Deflection Coil. Q114 provides relatively constant current to Q215 to optimize its operation.



P/O A4 DEFLECTION AMPLIFIER & STORAGE BOARD

FIG 6-27 DEFLECTION AMPLIFIERS

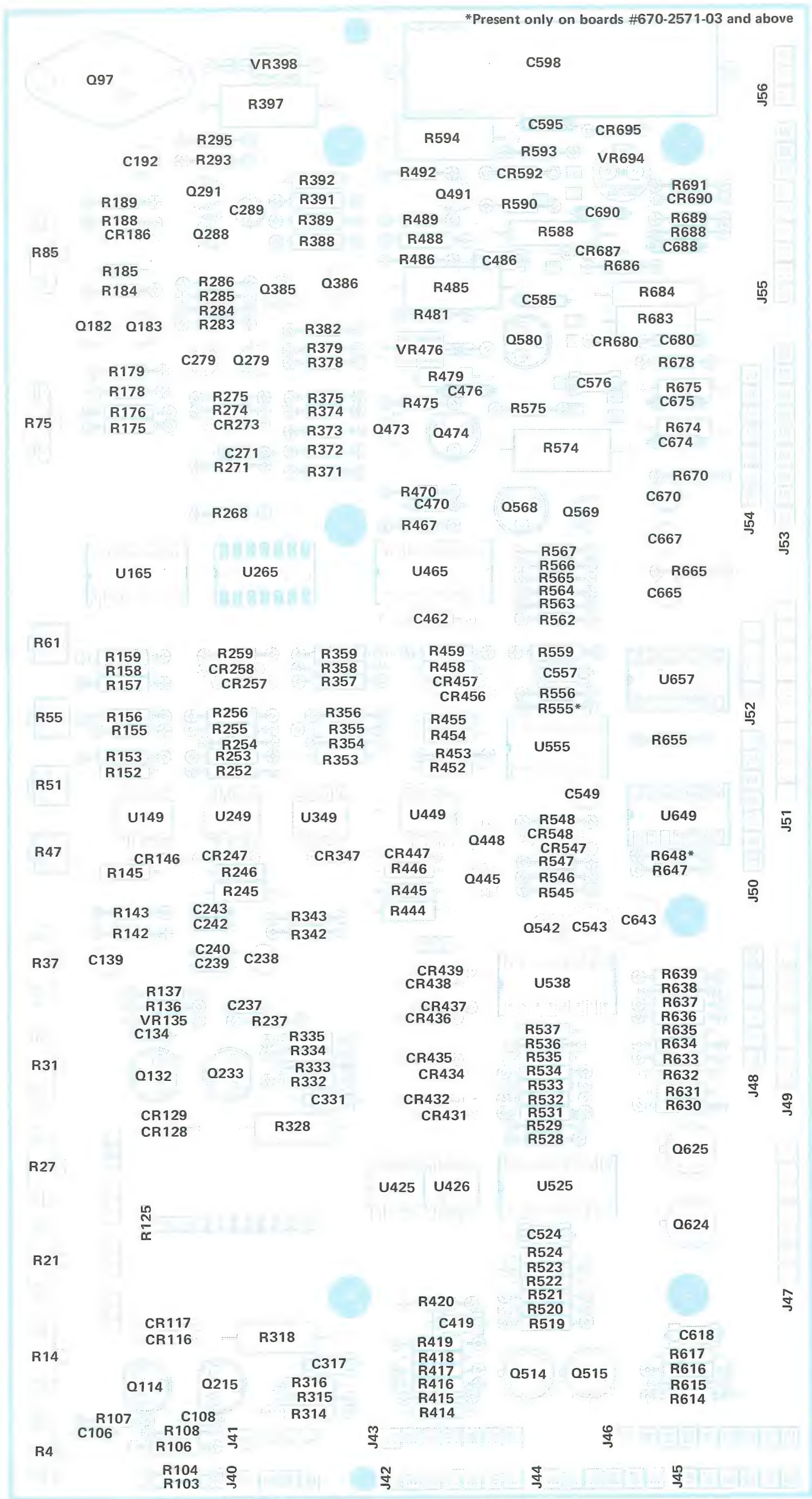


Fig. 6-26A. Deflection Amp and Storage Component Locations. Board #670-2571-03.

Ⓐ

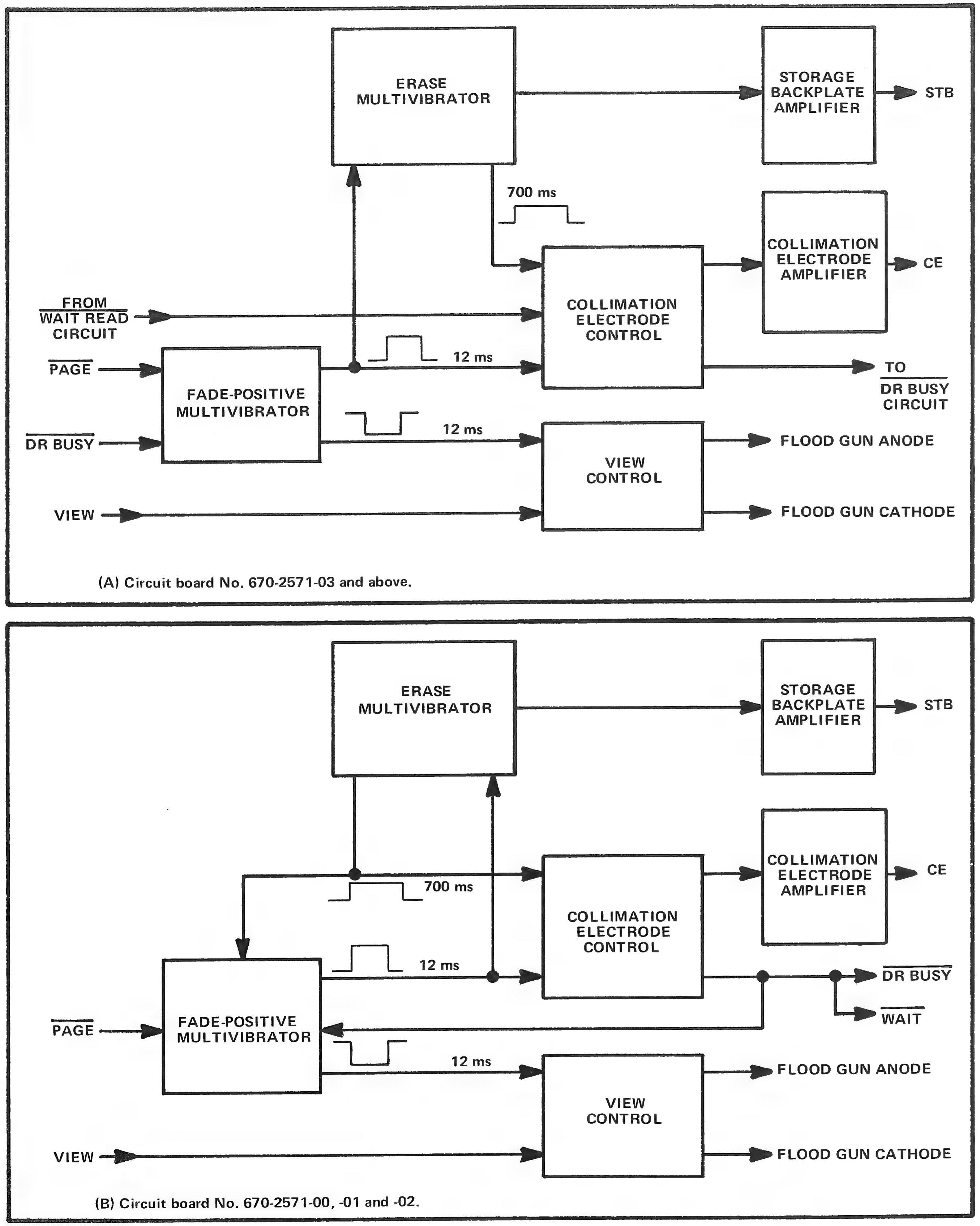
DEFLECTION AMPLIFIERS

CKT NO	GRID LOC
CAPS	
C106	B5
C108	A5
C134	B5
C139	D2
C237	B5
C238	C5
C239	D2
C240	A5
C242	D1
	D2
C243	D1
	D2
C317	B5
C331	C5
C419	B4
C524	D4
C543	D1
C618	B3
C643	D1
	C1
DIODES	
CR116	A5
CR117	A5
CR128	C5
CR129	C5
VR135	B5
CR431	A2
CR432	A2
CR434	A2
CR435	A2
CR436	C2
CR437	C2
CR438	C2
CR439	C2
TRANSISTORS	
Q114	A5
Q132	C5
Q215	A5
Q233	B5
	C5
Q514A	B3
Q514B	B4
Q515A	C3
Q515B	C4
Q624A	A3
Q624B	A3
Q625A	C3
Q625B	C2
Q1040	A5
Q1042	A5
Q1044	C5
Q1046	C5
RESISTORS	
R4	A4
R14	B5
R21	B4
R27	D4
R31	D5
R37	C4

CKT NO	GRID LOC
RESISTORS	
R106	A4
R107	A5
R108	A5
R125A	A5
R125B	A5
R125C	B5
R125D	B5
R125E	D5
R125F	D5
R125G	C5
R125H	C5
R136	B4
	B5
R137	C5
R142	D2
R143	D2
R237	B5
R314	A4
R315	B4
R316	B5
R318	A5
R328	C5
R332	D5
R333	B4
R334	B4
R335	C4
R342	D2
R343	D2
R414	B3
R415	B3
R416	B3
R417	B3
R418	B4
R419	B4
R420	B4
R519	A3
	B3
R520	C3
R521	C3
R522	D3
R523	D4
R524	D4
R528	A3
R529	A2
R531	A2
R532	A3
R533	A2
R534	B2
R535	B2
R536	A2
R537	A2
R614	C3
R615	C3
R616	B3
R617	C3
R630	C3
R631	A3
R632	C2
R633	C2
R634	C3
R635	C2
R636	C2
R637	C2
R638	C2
R639	C2

CKT NO	GRID LOC
IC's	
U425	A4
	A5
U426	B4
	B5
	C4
	C5
U525A	B4
U525B	C4
	D4
U525C	A3
U538A	A2
U538B	A2
U538C	C2
U538D	C2

Ⓐ



(A) Circuit board No. 670-2571-03 and above.

(B) Circuit board No. 670-2571-00, -01 and -02.

Fig. 6-28. Storage Circuit Block Diagram.

Ⓐ

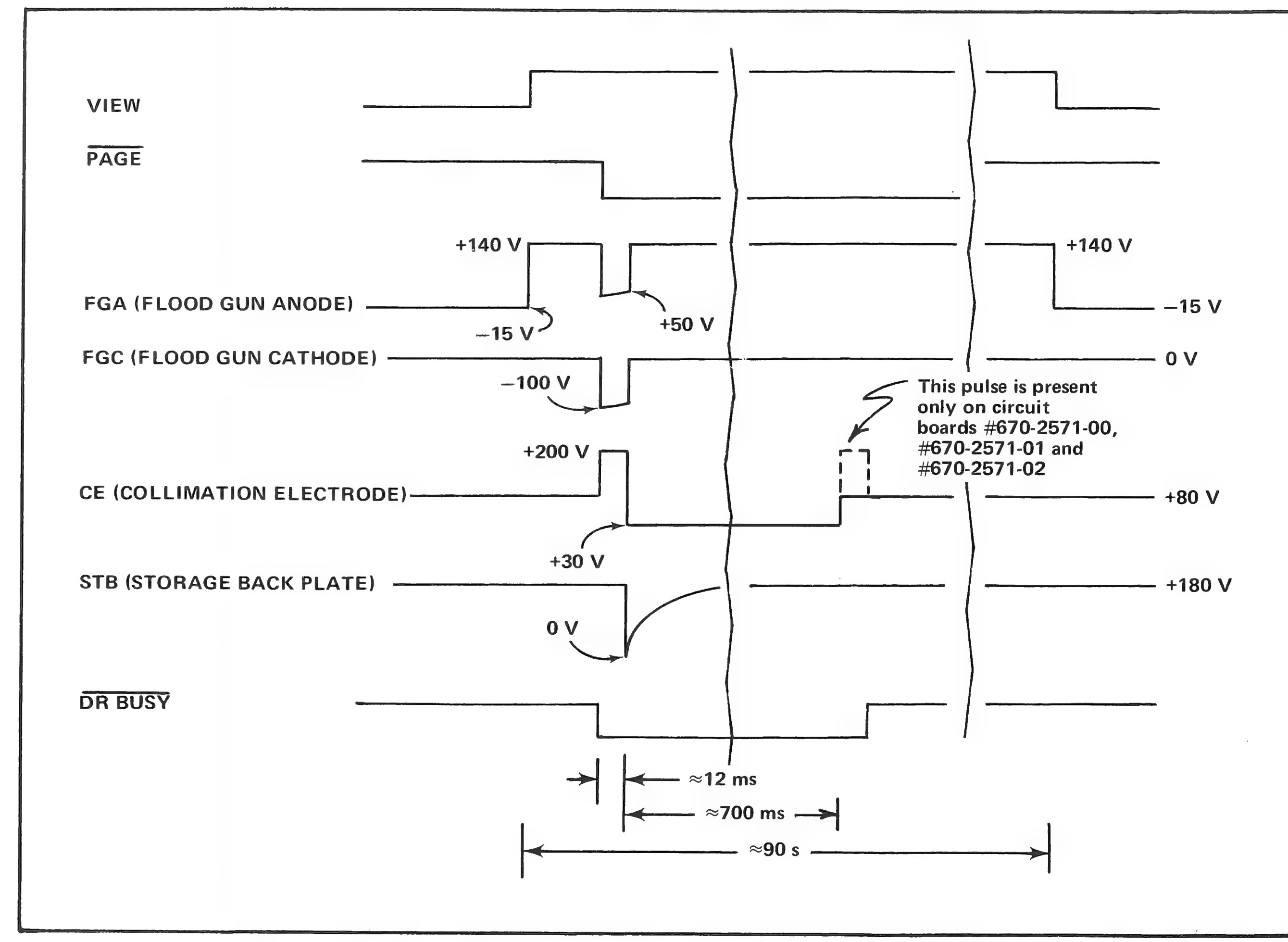


Fig. 6-29. Storage Circuit Waveforms.

Ⓐ

Storage Circuits

Block Diagram Description. The Storage circuit controls the storage and erasure of data on the face of the CRT. The Storage circuit consists of the following sections: The Fade-Positive Multivibrator, the Erase Multivibrator, Storage Backplate Amplifier, Collimation Electrode Control, Collimation Electrode Amplifier, and View Control.

A block diagram of the circuit is shown in Fig. 6-28A. Waveforms associated with the circuit's operation appear in Fig. 6-29.

The sequence that causes erasing starts with the low-going $\overline{\text{PAGE}}$ signal arriving at the Fade-Positive Multivibrator. If view is not already high, it will be sent high by the $\overline{\text{PAGE}}$ signal (in another circuit). Note that when VIEW goes high, the Flood Gun Anode voltage rises to +140 V, its normal viewing and writing level. $\overline{\text{PAGE}}$ causes a 12 millisecond low pulse to go to the View Control circuit, causing the anode and cathode to decrease their voltage by approximately 100 volts as shown in the waveform diagram. Simultaneously, the Fade-Positive Multivibrator applies a 12 millisecond high pulse to the Collimation Electrode Control circuit, where it initiates a negative-going $\overline{\text{DRBUSY}}$ signal. $\overline{\text{DRBUSY}}$ is applied to the Fade-Positive Multivibrator to disable it until the erase cycle is completed. The 12 ms high pulse also causes the Collimation Electrode Amplifier to generate a 12 millisecond positive-going pulse on the Collimation Electrode Line.

When the 12 millisecond pulse from the Fade-Positive Multivibrator ends, the anode and cathode voltages from the View Control circuit return to their quiescent value. The negative transmission into the Erase Multivibrator causes a signal to return to the Collimation Electrode Control to sustain the $\overline{\text{DRBUSY}}$ signal and to change the Collimation Electrode Voltage to a value below that which occurs at quiescence. At the same time, the Erase Multivibrator causes the Storage Backplate Amplifier to drive the Storage Backplate Voltage (STB) to zero, from where it rises exponentially toward its previous voltage.

The signal from the Erase Multivibrator ends after approximately 700 milliseconds, causing the Collimation Electrode Control to set the Collimation Electrode Voltage back to its quiescent value. $\overline{\text{DRBUSY}}$ continues to be held low for a short additional time.

A block diagram for early-version boards appears in Fig. 6-28B. It is similar to that just discussed, differing principally in the $\overline{\text{DRBUSY}}$ circuit.

Refer to the waveform diagram in Fig. 6-29. The positive-going Collimation Electrode Voltage and the negative-going voltage on the Flood Gun Anode and Cathode together cause flooding of the CRT Faceplate, providing uniform storage over the entire area. After the 12 millisecond pulse elapses, the collimation electrode returns to a value lower than quiescence to prevent any storing from occurring until the end of the cycle. At the same time that the voltage pulses end, the Storage Backplate Voltage goes to zero to erase the face of the CRT. 700 milliseconds later, the Storage Backplate Voltage has returned to normal; the Collimation Electrode Voltage returns to normal. The $\overline{\text{DRBUSY}}$ signal returns high after a short additional period, indicating that erasing has been completed.

Detailed Description. Refer to the schematic of the Storage circuit, Fig. 6-31 or Fig. 6-31A, as applies to the specific board being considered. The Erase Multivibrator and Storage Backplate Control Amplifier (which determine the backplate voltage) will be discussed first. Under quiescent conditions, −15 volts is applied through R189, R188 and CR186 to hold Q288 in conduction. This causes Q291 to be in conduction with approximately −14.8 volts on its collector. The voltage at the R189, R188 junction is approximately −2.4 volts, causing C192 to charge approximately 12.4 volts. The base of Q183 is held at approximately −1.2 volts by the Q288 base-to-emitter junction and by CR186. This holds the emitter of Q183 at −1.8 volts, which holds the emitter of Q182 at −1.2 volts. Referring to Q474, it can be seen that its emitter holds its base at approximately +0.6 volt, holding the base of Q473 at zero volts. 1.2 volts thus exists between the emitter of Q182 and the base of Q473. With the Op Level control at mid-position, about 1/3 of a milliampere flows between the emitter of Q182 and the base of Q473. Very little of this passes through the Q473 base-emitter junction, leaving the majority of it to flow through R684. Multiplying this 1/3 milliampere by the R684 value (499 kΩ) provides approximately +180 volts at the emitter of Q532. The Q473, Q474, Q1030, and Q1032 circuit serves as a driver amplifier to sustain this voltage. The +180 volts at the emitter of Q1032 is felt at the Storage Backplate (STB) anode of the CRT.

After $\overline{\text{PAGE}}$ has been applied to U465B and the 12 millisecond multivibrator pulse expires, the negative transition is felt through C271 into Q291, turning this

transistor off. Its collector goes toward zero volts. Since C192 has a 12.5 volt charge on it, the right side of this capacitor goes positive and the capacitor attempts to discharge through R293-R189. The C192-R189 junction rises to approximately 12 volts and turns Q288 off. With Q288 cut off, its collector goes toward −15 volts, holding Q291 cut off. The positive voltage at the CR186-R188 junction is felt through the base-emitter circuit of Q183 and the emitter-base circuit of Q182. The positive potential at the emitter of Q182 causes zero volts to appear at the R176-R175 junction. With zero volts at the base of Q473, no current is demanded through R75, and therefore none flows through R684. This causes the operational amplifier to place a zero volt output on the Storage Backplate (STB) anode.

During the next 700 ms, C192 discharges exponentially, changing the voltage being applied to the base of Q183. The STB voltage changes toward 180 V. After approximately 700 milliseconds, C192 discharges to the point where the voltage at the cathode of CR186 drops to about −1 volt, causing it and Q288 to go back into conduction. When this happens, the Storage Backplate voltage has been returned to its quiescent level. With Q288 in conduction, Q291 goes back into conduction, permitting C192 to again charge to its quiescent value.

This paragraph applies only to circuit boards 670-2571-03 and above. The Collimation Electrode circuit will be discussed next. Under quiescent conditions, both inputs to U265D are low, placing a low at Pin 8 of U265C. The low from U465B pin 5 is also applied to U265A, pin 2. The second inputs to U265C and U265A are supplied by a Hard Copy circuit and are low except during copy making. The U265C output is therefore high, holding Q385 cut off. With Q385 cut off, the circuit connected to its collector circuit delivers about one-third of a milliampere of current to the null point at the base of Q491 in the Collimation Electrode Amplifier.

This paragraph applies only to circuit boards 670-2571-00, -01, and -02. The Collimation Electrode circuit will be discussed next. Under quiescent conditions, both inputs to U265D are low, placing a low at pin 8 of U265C. This same low occurs at pin 5 of U265B and is applied to R169. The low at R169 causes a high out of U165D. The U265B output remains low, causing a second low to be applied to U265C. The U265C output is therefore high, holding Q385 cut off. With Q385 cut off, the circuit connected to its collector circuit delivers about one-third of a milliampere of current to the null point at the base of Q491 in the Collimation Electrode Amplifier.

The two low inputs to U265A cause a low out of U165C; Q386 is turned on. This holds about −0.2 V on the Q386 collector, delivering about 0.3 mA to the null point at Q491. In addition, R488 current flows into this point and is equal to about 0.25 mA. The combined currents flowing through R588 cause the output of the operational amplifier to be at approximately 80 volts.

When $\overline{\text{PAGE}}$ is received and the pin 5 output of U465B goes high, U265D, U165A, and U165D cause $\overline{\text{DRBUSY}}$ to occur. This is routed back to disable U465B so that no additional $\overline{\text{PAGE}}$ signals can affect the circuit until the erase cycle ends. Highs appear at the pin 8 input of U265C and pin 2 input of U265A. This causes Q385 to turn on and Q386 to turn off. The emitter circuit of Q385 now delivers about 0.13 mA, to the base of Q491. Again, this current combines with that from R488 and flows through R588, causing the output of Q1036 to reach approximately 200 volts, which is applied to the Collimation Electrode of the CRT. When the 12 millisecond pulse from U465B expires, the high is removed from pin 2 of U265A, causing Q386 to go into conduction. Since Q279 (in the Erase Multivibrator circuit) delivers a high to pin 11 of U265D, a high is maintained on pin 8 of U265C, holding Q385 in conduction. With both transistors in conduction, Q385 delivers about 0.13 mA while Q386 delivers about .03 mA. These combine with the 0.25 mA from R488. The current through R588 causes the Collimation Electrode Voltage to drop to approximately 30 volts.

This paragraph pertains only to circuit boards 670-2571-03 and above. The just-described situation continues until the 700 ms erase period ends, and Q270 is again put in conduction. At this time, pin 11 of U265D goes low, applying a low at pin 8 of U265C, and at pin 9 of U165D. The high at pin 8 of U265C permits the Collimation Electrode Control and the Collimation Electrode Voltage Amplifier circuits to return to quiescent operating conditions. Although the output of U165D goes high, $\overline{\text{DRBUSY}}$ remains low for a short period. (This is due to C549, shown on the Hard Copy Selector schematic.) Note that the effect of the $\overline{\text{WAIT}}$ and $\overline{\text{READ}}$ signals are applied to inputs of U265C and U265A. When a Hard Copy request occurs, the outputs of those devices go low. This causes the Collimation Electrode Voltage to go to +200 Volts during Hard Copy operation.

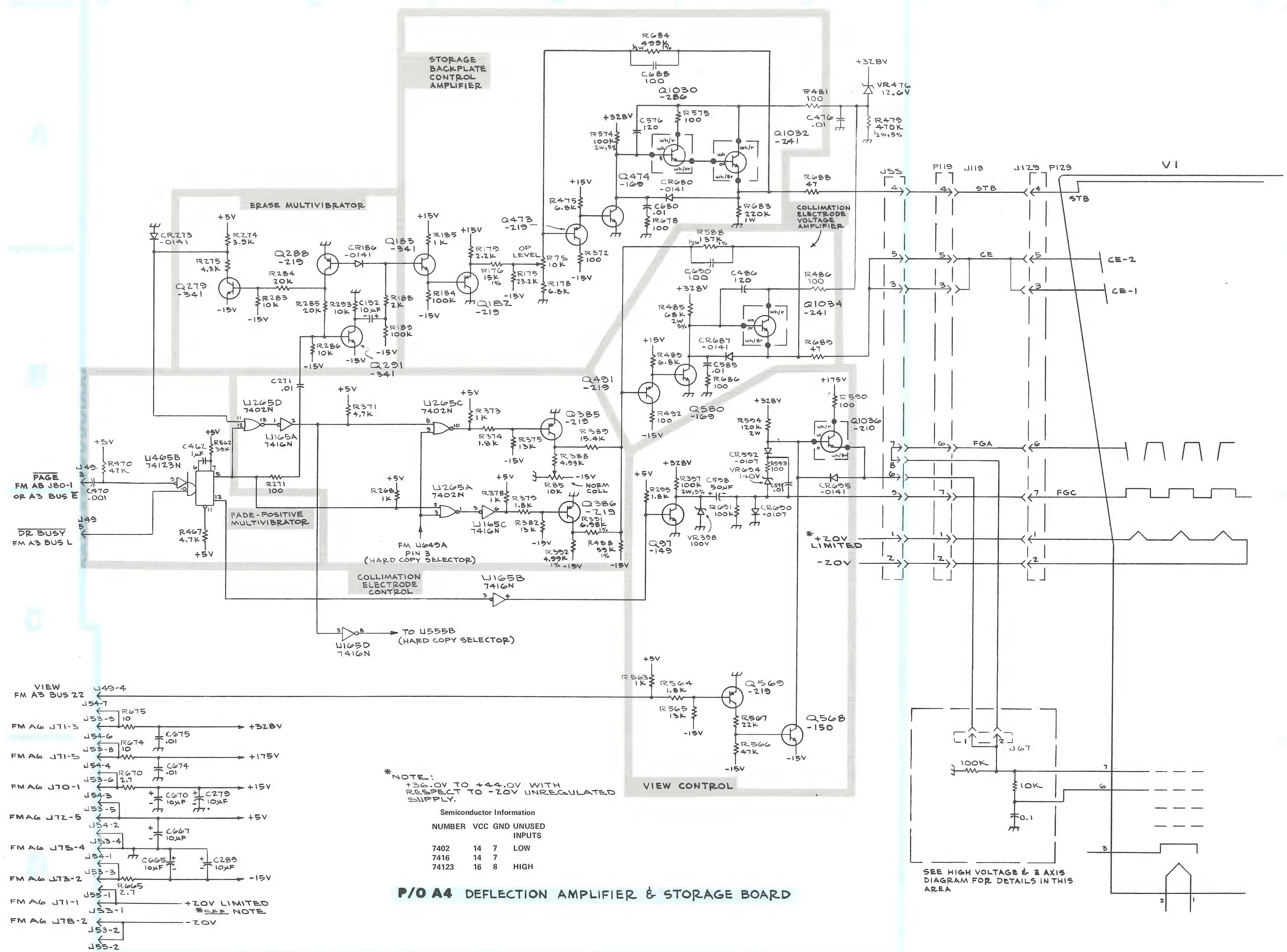
This paragraph pertains only to circuit boards 670-2571-00, -01, and -02. The just-described situation continues until the 700 ms erase period ends, and Q279 is again put in conduction. At this time, pin 11 of U265D goes low, applying a low on pin 8 of U265C and pin 5 of

U265B. The low from the collector of Q279 is also applied to U465A, which delivers a 12 millisecond pulse to pin 6 of U265B. With lows on pin 5 and pin 6, U265B places a high on U265C and U265A. This causes Q385 to go into conduction and Q386 to turn off. The Collimation Electrode Voltage now rises to approximately 200 volts, where it remains until U465A ends its 12 millisecond pulse. Then a high is placed at pin 6 of U265B, putting a low into U265A and U265C. The outputs of these two devices return high, causing Q385 to turn off and Q386 to conduct. This restores the Collimation Electrode to its quiescent operating value of approximately 80 volts. Note that the U265D output was low throughout the time the high 12 milliseconds pulse was being emitted by pin 5 of U465B and during the time that Q279 was cut off. This causes U165A to apply a high to R169, charging C169. The resulting low from U165D held $\overline{\text{DRBUSY}}$ low, indicating that the CRT was erasing. In addition, when the collector of Q279 went low, it caused U465A to create a 12 millisecond pulse that extended the low $\overline{\text{DRBUSY}}$ signal by that amount. Notice that the $\overline{\text{WAIT}}$ signal inputs to the positive input of U465B and also holds the pin 6 input of U265B low. $\overline{\text{WAIT}}$ originates from the Hard Copy Unit (from those Hard Copy Units equipped with the Multiplexer option) and is used here to prevent an erase function during the time $\overline{\text{WAIT}}$ is active. (See the description of the $\overline{\text{WAIT}}$ signal in the Detailed Circuit Description of the Hard Copy Circuits.)

The View Control circuit quiescently holds the Flood Gun Cathode at approximately zero volts and the anode at about 140 volts. A voltage divider in the base of Q1036 includes diode CR690, which conducts to hold the cathode near zero volts. Zener diode VR694 conducts to raise the voltage at the base of Q1036 to approximately +140 volts. This is felt through the base-to-emitter circuit of Q1036, where it is applied to the anode of the flood guns. Since U465B (in the Fade-Positive Multivibrator) has its pin 12 high under quiescent conditions, U165B delivers a low to the base of Q97, holding that transistor cut off. Zener diode VR398 conducts and causes +100 volts to be placed on the left plate of C598. With anode of CR690 very near ground potential, C598 charges to approximately 100 volts.

When a $\overline{\text{PAGE}}$ signal is received, pin 12 of U465B goes low, causing U165B to deliver a high to the base of Q97. This transistor conducts and places the left plate of C598 near ground potential. With the left plate going negative by 100 V, the right plate is driven negative by an equal amount, placing a −100 V signal on the cathode of the flood guns. Since VR694 is still conducting, the voltage on the base of Q1036 drops to +40 V. The cathode of Q1046 and the CRT flood gun anode are thus caused to change in step with the CRT cathode voltage. After the 12 ms pulse from U465B elapses, the voltages return to their previous levels, 0 and +140 volts.

Under viewing conditions, the VIEW signal is high, holding Q569 cut off, which holds Q568 cut off and permits the just-described situation to exist. However, when the viewing period has elapsed and the VIEW signal goes low, Q569 goes into conduction, causing Q568 to conduct. This back-biases CR592 and places approximately −15 volts on the base of Q1036. The Q1036 emitter voltage and flood gun anode voltage drop to about −15.6 V. With the flood gun cathode at 0 V, the flood gun decreases conduction and drops the CRT intensity below the viewing level.



*NOTE:
+36.0V TO +44.0V WITH RESPECT TO -20V UNREGULATED SUPPLY.

Semiconductor Information

NUMBER	VCC	GND	UNUSED INPUTS
7402	14	7	LOW
7416	14	7	
74123	16	8	HIGH

P/O A4 DEFLECTION AMPLIFIER & STORAGE BOARD

FIG 6-31 STORAGE CIRCUIT
DAS BOARD # 670-2571-03

Ⓐ

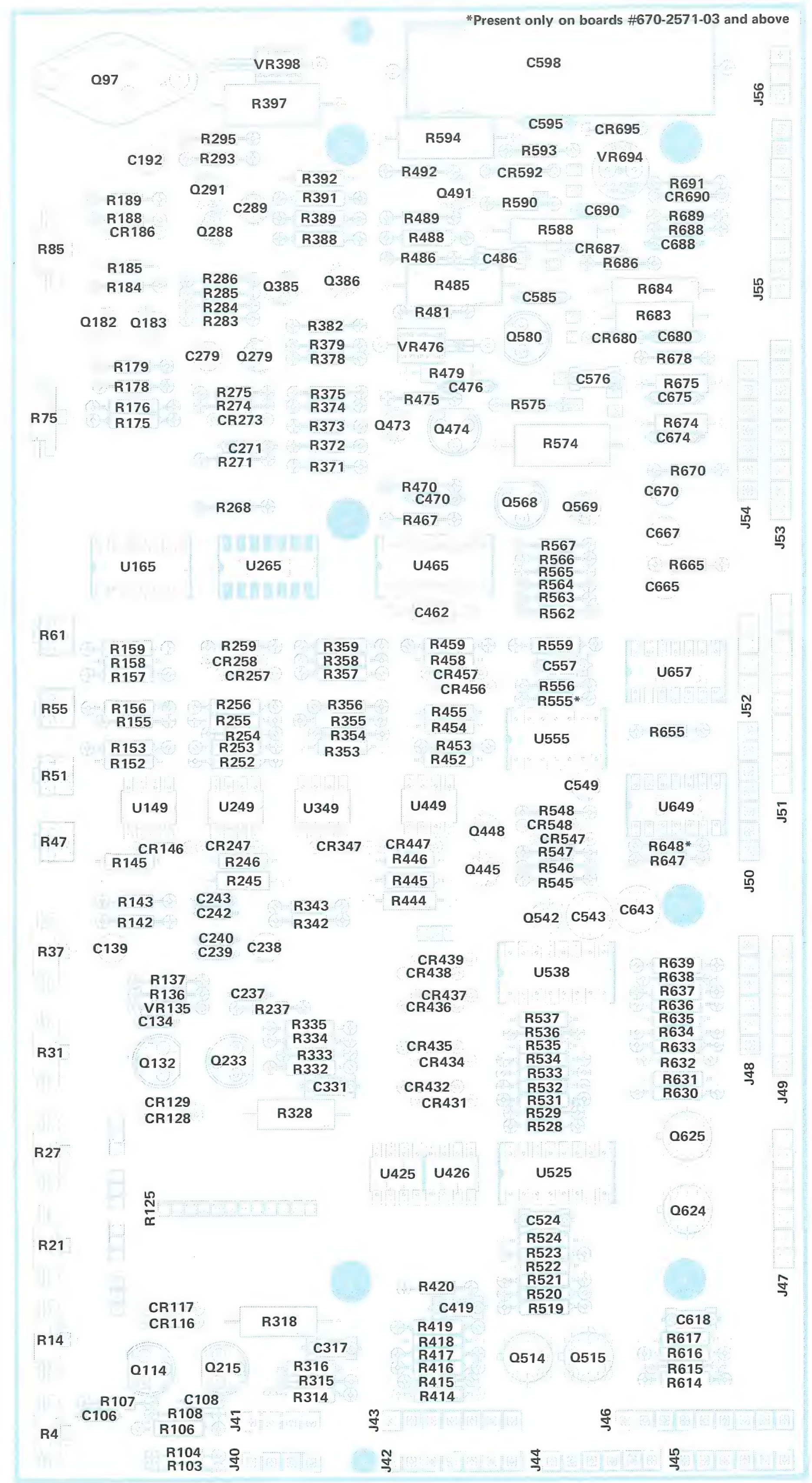


Fig. 6-30. Deflection Amp and Storage Component Locations. Board #670-2571-03.

Ⓐ

STORAGE CIRCUIT

CKT NO	GRID LOC
CAPS	
C169	C2
C192	B2
C271	B2
C279	D2
C289	D2
C462	B2
C470	B1
C476	A4
C486	B4
C576	A3
C585	B4
C595	B4
C598	C4
C665	D1
C667	D1
C670	D1
C674	D1
C675	D1
C680	A3
C688	A3
C690	B4
DIODES	
CR186	B2
CR273	A1
VR398	C4
VR476	A4
CR592	B4
CR680	A3
CR687	B4
CR690	C4
VR694	B4
CR695	B4
TRANSISTORS	
Q97	C3
Q182	B3
Q183	B2
Q279	B2
Q288	B2
Q291	B2
Q385	B3
Q386	C3
Q473	A3
Q474	A3
Q491	B3
Q568	C4
Q569	C4
Q580	B4
Q1030	A3
	A4
Q1032	A4
Q1034	B4
Q1036	B4
IC's	
U165A	B2
U165B	C3
U165C	C3
U165D	C2
U265A	C3
U265C	B3
U265D	B2
U465B	B2

CKT NO	GRID LOC
RESISTORS	
R75	B3
R85	B3
R175	B3
R176	B3
R178	B3
R179	B3
R184	B2
R185	A2
R188	B2
R189	B2
R268	B2
R271	B2
R274	A2
R275	B2
R283	B2
R284	B2
R285	B2
R286	B2
R293	B2
R295	B3
	C3
R371	B2
R372	B3
R373	B3
R374	B3
R375	B3
R378	C3
R379	C3
R382	C3
R388	B3
R389	B3
R391	C3
R392	C3
R397	B3
	B4
R467	C2
R470	B1
R475	A3
R479	A4
R481	A4
R485	B4
R486	B4
R488	C3
R489	B3
R492	B3
R562	B2
R563	C3
R564	C3
	C4
R565	C4
R566	D4
R567	C4
R574	A3
R575	A3
R588	A4
R590	B4
R593	B4
R594	B4
R665	D1
R670	D1
R674	D1
R675	C1
R678	A3
R683	A4
R684	A3
R686	B4
R688	A4
R689	B4
R691	C4

Ⓐ

STORAGE CIRCUIT
(BOARD NO.
670-2571-00, 01 & 02)

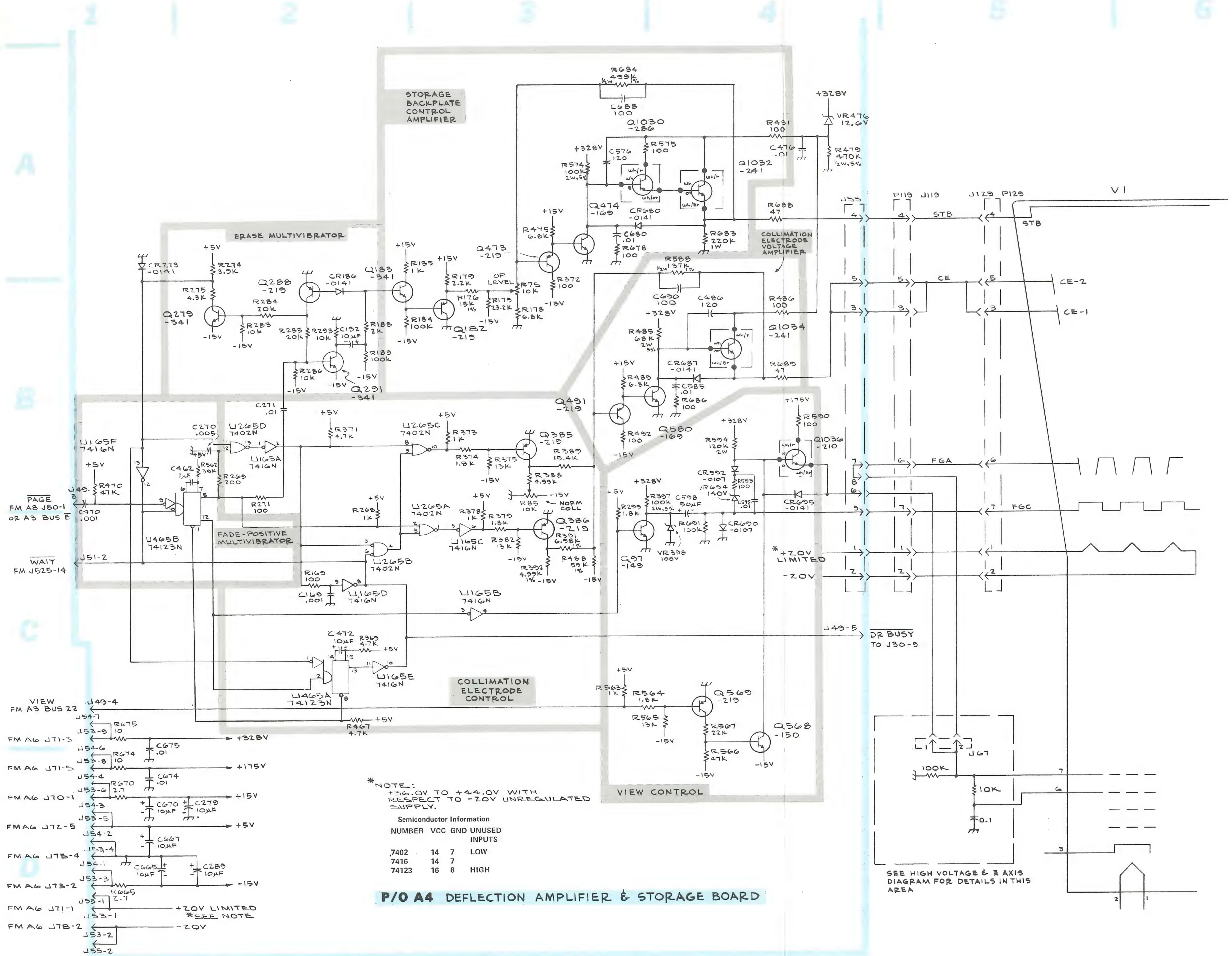


FIG 6-31A STORAGE CIRCUIT
DAS BOARD # 670-2571-00, 670-2571-01, 670-2571-02

Ⓐ

STORAGE CIRCUIT

CKT NO	GRID LOC	CKT NO	GRID LOC	CKT NO	GRID LOC
CAPS		RESISTORS		RESISTORS	
C169	C2	R75	B3	R590	B4
C192	B2	R85	B3	R593	B4
C270	B2	R169	C2	R594	B4
C271	B2	R175	B3	R665	D1
C279	D2	R176	B3	R670	D1
C289	D2	R178	B3	R674	D1
C462	B2	R179	B3	R675	C1
C470	B1	R184	B2	R678	A3
C472	C2	R185	A2	R683	A4
C476	A4	R188	B2	R684	A3
C486	B4	R189	B2	R686	B4
C576	A3	R268	B2	R688	A4
C585	B4	R269	B2	R689	B4
C595	B4	R271	B2	R691	C4
C598	C4	R274	A2		
C665	D1	R275	B2		
C667	D1	R283	B2	IC's	
C670	D1	R284	B2		
C674	D1	R285	B2	U165A	B2
C675	D1	R286	B2	U165B	C3
C680	A3	R293	B2	U165C	C3
C688	A3	R295	B3	U165D	C2
C690	B4		C3	U165E	C2
		R369	C2	U165F	B1
DIODES		R371	B2	U265A	C3
		R372	B3	U265B	C2
CR186	B2	R373	B3	U265C	
CR273	A1	R374	B3	U265D	B2
VR398	C4	R375	B3	U465A	C2
VR476	A4	R378	C3	U465B	B2
CR592	B4	R379	C3		
CR680	A3	R382	C3		
CR687	B4	R388	B3		
CR690	C4	R389	B3		
VR694	B4	R391	C3		
CR695	B4	R392	C3		
		R397	B3		
TRANSISTORS			B4		
		R467	C2		
Q97	C3	R470	B1		
Q182	B3	R475	A3		
Q183	B2	R479	A4		
Q279	B2	R481	A4		
Q288	B2	R485	B4		
Q291	B2	R486	B4		
Q385	B3	R488	C3		
Q386	C3	R489	B3		
Q473	A3	R492	B3		
Q474	A3	R562	B2		
Q491	B3	R563	C3		
Q568	C4	R564	C3		
Q569	C4		C4		
Q580	B4	R565	C4		
Q1030	A3	R566	D4		
	A4	R567	C4		
Q1032	A4	R574	A3		
Q1034	B4	R575	A3		
Q1036	B4	R588	A4		

Ⓐ

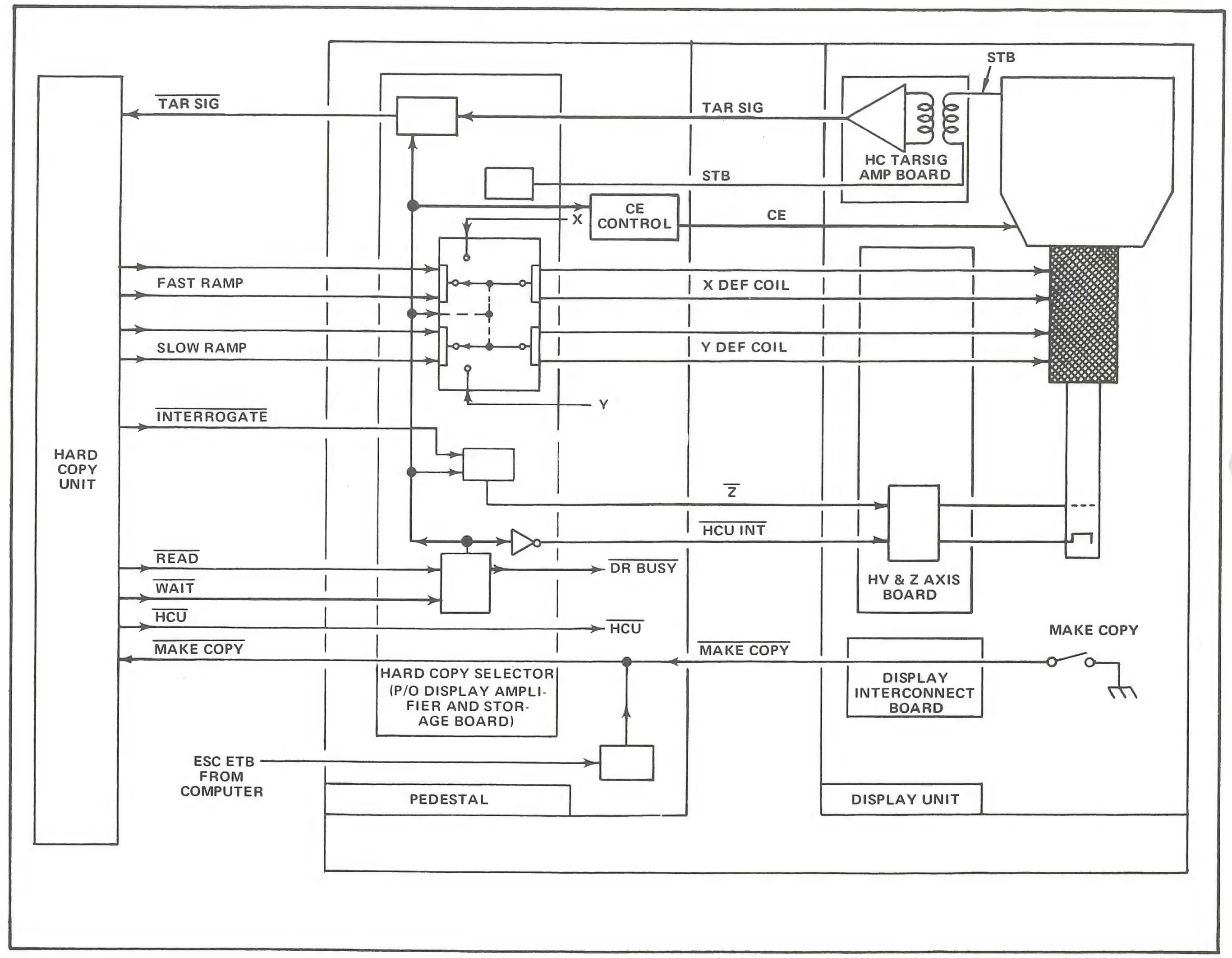


Fig. 6-32. Hard Copy Operation Block Diagram.

Ⓐ

Hard Copy Circuits

Block Diagram Description. The overall purpose of the Hard Copy Selector is to provide the Hard Copy Unit with a command for initiating a hard copy, then supplying the Hard Copy Unit with writing information that represents the data stored on the CRT.

Refer to Fig. 6-32. Whenever the Hard Copy Unit is attached and energized, an HCU signal is presented to the Terminal to advise of its availability. Whenever a MAKE COPY signal is initiated at the Display Unit, or is initiated by an ESC ETB sequence from the computer, the MAKE COPY command is applied to the Hard Copy Unit where it causes several outputs. A READ signal and a WAIT signal are applied to the Terminal to indicate that a hard copy is being made. This causes the Terminal to generate a DRBUSY signal to disable keyboard and computer inputs to the Terminal. The Terminal also generates an HCU INT signal to modify the cathode and control grid voltages of the Display Unit writing circuits. READ causes the Deflection circuits to select X and Y inputs from the Hard Copy Unit rather than from the Terminal circuits. In addition, the READ signal causes enabling voltages to be placed on the Z Axis circuit and the TARSIG circuits within the Deflection Amplifier and Storage board. The CE Voltage to the Storage circuits is also modified by the READ signal effects, adjusting the display to an intensity compatible with copy making.

The Hard Copy Unit provides a positive-going slow ramp to the Y Deflection circuits in the Terminal to cause the Terminal to sweep vertically one time. As it sweeps, a succession of fast ramps is supplied to the X Deflection circuits. This causes repetitive horizontal sweeps during the vertical sweep. The ramp signals are supplied to the Readout circuits in the Hard Copy Unit at the same time they are being provided to the Terminal, permitting both units to be evaluating the same point on the display.

During each fast ramp, the Hard Copy Unit supplies repetitive INTERROGATE signals to the Terminal. These cause Z signals to be sent from the Deflection Amp and Storage board to the High Voltage & Z Axis board in the Display Unit. There they turn the writing beam on. If writing exists on the storage backplate in the position indicated by the deflection coils, the resultant current in the Storage Backplate circuit causes a TARSIG signal to be generated on the Hard Copy TARSIG Amplifier board. This is sent to the Pedestal section where it is gated through by the READ signal. This results in TARSIG being sent to the Hard Copy Unit. The Hard Copy Unit then writes a point at the position commanded by the fast and slow ramps. When the slow ramp ends, Hard Copy operation is discontinued and all signal lines except HCU return to their inactive status. Control of the Deflection circuit is returned to the X and Y signals from the Terminal.

Detailed Circuit Description. Refer to the Hard Copy Selector schematic, Fig. 6-34. The X and Y outputs are each the output of one of two amplifiers, as selected by the Q448 circuit. With Hard Copy not selected, the WAIT and READ signals are high, placing a high on the base of Q445 via Q542. This causes Q448 to place lows at the CR258-CR257 and the CR457-CR456 junctions. CR258 and CR457 are forward-biased, placing lows at the positive inputs of U149 and U349. Their outputs are driven sufficiently low to back-bias CR146 and CR347, disconnecting the amplifiers from the output circuit. At the same time, diodes CR257 and CR456 become back-biased, preventing Q448 from affecting either U249 or U449. This permits the X and Y signals to control the X and Y outputs to the Deflection Amplifier circuit. Each amplifier has a gain of approximately one.

When a Hard Copy is commanded, READ goes low, causing the emitter of Q448 to go high. This places highs at the negative inputs of U249 and U449, causing their outputs to go low. CR247 and CR447 become back-biased, preventing U249 and U449 from affecting the X and Y outputs. CR258 and CR457 are also reverse-biased, permitting the FAST RAMP and SLOW RAMP to control the X and Y outputs to the Deflection Amplifiers. The output amplitudes can be controlled by adjusting R51 and R61, which determine the amount of voltage being presented to the amplifiers. R47 and R55 provide X and Y positioning adjustments for the Fast and Slow ramps, respectively. A strap option on the Deflection Amplifier schematic permits the X and Y Deflection Amplifiers to both be controlled by the Y signal. This permits simultaneous application of equal drive signals to both axes for calibration purposes.

This paragraph pertains only to board No. 670-2571-03 and above. U649A also controls U649D, U465A, U657B, and U657C. When READ and WAIT are high, the outputs of these circuits rest at their inactive state. When READ or WAIT go low, the following happens: HC INT goes low, DRBUSY goes low, TARSIG is put under the control of the TARSIG input signal, and Z is placed under the control of INTERROGATE; U465A causes a Z pulse to occur in response to each INTERROGATE signal. When READ or WAIT return high, C549 holds a low on U555A for a short time, holding DRBUSY low for that additional period. The WAIT signal is an input from the Hard Copy Unit (if the

Hard Copy Unit is equipped with the Multiplexer option). If the Hard Copy Unit is copying another Terminal's display, the $\overline{\text{WAIT}}$ signal holds the waiting Terminal inactive until the Hard Copy Unit gets around to copying its display. When the copy is completed, $\overline{\text{WAIT}}$ and $\overline{\text{READ}}$ go inactive.

This paragraph pertains only to board No. 670-2571-00, -01, and -02. The $\overline{\text{READ}}$ signal also controls U555B, U649D, U555A, U657B, and U657C. When $\overline{\text{READ}}$ is high, the outputs of these circuits rest at their inactive state. When $\overline{\text{READ}}$ goes low, the following happens: $\overline{\text{HC INT}}$ goes low, $\overline{\text{DRBUSY}}$ goes low, $\overline{\text{TARSIG}}$ is put under the control of the TARSIG input signal, and $\overline{\text{Z}}$ is placed under the control of $\overline{\text{INTERROGATE}}$. While $\overline{\text{READ}}$ is low, U555A causes a $\overline{\text{Z}}$ pulse (0.2 to 0.6 μs, variable) to occur in response to each $\overline{\text{INTERROGATE}}$ signal. When $\overline{\text{READ}}$ returns high, C654 holds a low on pin 9 of U649C while U555B places a 150 microsecond low on pin 10 of U649C, holding $\overline{\text{DRBUSY}}$ low for that additional period. The $\overline{\text{WAIT}}$ signal is an input from the Hard Copy Unit (if the Hard Copy Unit is equipped with the Multiplexer option). When the Terminal issues a Make Copy request, the Hard Copy Unit responds to the Terminal with the $\overline{\text{WAIT}}$ signal. $\overline{\text{WAIT}}$ is used to hold $\overline{\text{DRBUSY}}$ active until the Hard Copy Unit has completed making the copy. When the copy is completed, $\overline{\text{WAIT}}$ and $\overline{\text{READ}}$ go inactive. $\overline{\text{READ}}$ going inactive, causes U555B to fire, thus extending $\overline{\text{DRBUSY}}$ as explained in the preceding paragraph.

Refer to the Hard Copy TARSIG Amplifier schematic diagram, Fig. 6-36. The Hard Copy TARSIG Amplifier board permits the STB current to be monitored. Since this current reflects whether a written or non-written area is being scanned, it provides information for hard copy writing. Filtering is provided to the remaining CRT lines to minimize circuit noise.

The storage backplate signals are coupled through T38 and applied to differential amplifier U59, which has a gain of approximately 400. Its output is amplified by approximately 10 in U79 and applied to comparator U95. U95 provides a negative output pulse in response to STB signals of an amplitude determined by threshold potentiometer R167. R167 permits the voltage at the positive input of U95 to be set between 0 and +3.3 volts. The Dynamic Threshold adjustment (R265) provides a correction voltage that gives optimum uniformity of separation between the signal levels on TP85 and TP195 as the scanning signals monitor the entire screen area. This provides U95 with a more uniform pulse, regardless of where on the CRT the STB pulse originated. The U95 output pulses are applied to one-shot multivibrator U289, which responds by generating 0.4 μs (approximate) positive-going TARSIG pulses.

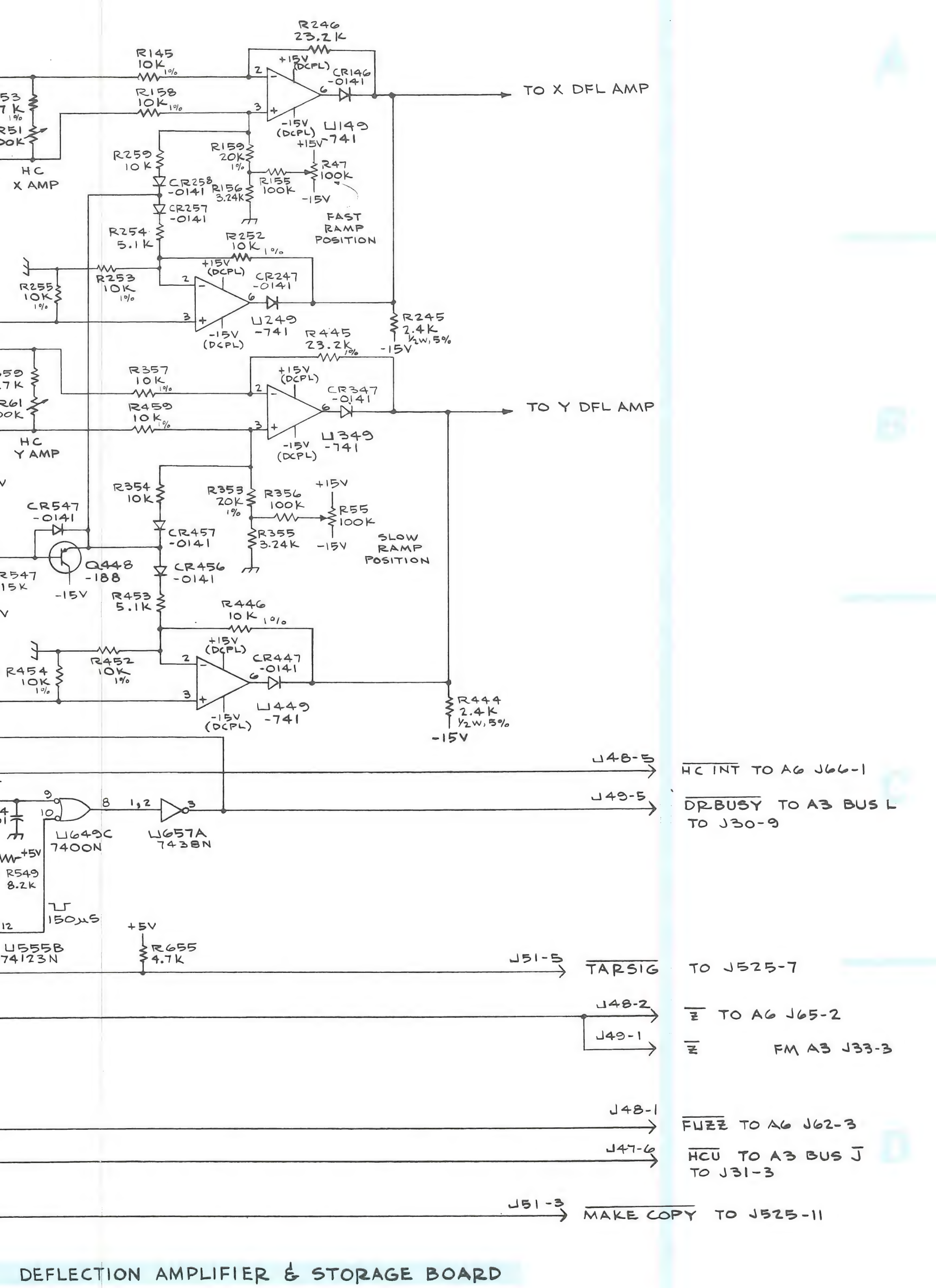


FIG 6-34A HARD COPY SELECTOR
DAS BOARD #670-2571-00, 670-2571-01, 670-2571-02

HARD COPY SELECTOR

CKT NO	GRID LOC
CAPS	
C549	C4
C557	D3
C654	C4
DIODES	
CR146	A5
CR247	B4
CR257	A4
CR258	A4
CR347	B5
CR447	C4
CR456	B4
CR457	B4
CR547	B4
CR548	C3
TRANSISTORS	
Q445	B4
Q448	B4
Q542	B3
RESISTORS	
R47	A5
R51	A4
R55	B5
R61	B4
R145	A4
R152	A4
R153	A4
R155	A4
R156	A4
R157	A4
R158	A4
R159	A4
R245	B5
R246	A5
R252	B4
R253	B4
R254	A4
R255	B4
R256	B4

CKT NO	GRID LOC
RESISTORS	
R259	A4
R353	B4
R354	B4
R355	B4
R356	B4
R357	B4
R358	B4
R359	B4
R444	C5
R445	B5
R446	C4
R452	C4
R453	B4
R454	C4
R455	C4
R458	B4
R459	B4
R545	B3
R546	B4
R547	B4
R548	C3
R549	C4
R556	D3
R559	D3
R647	C2
R654	C4
R655	C4
IC's	
U149	A4
U249	B4
U349	B4
U449	C4
U555A	D3
U555B	C4
U649A	C3
U649B	
U649C	C4
U649D	C3
U657A	C4
U657B	D3
U657C	D3

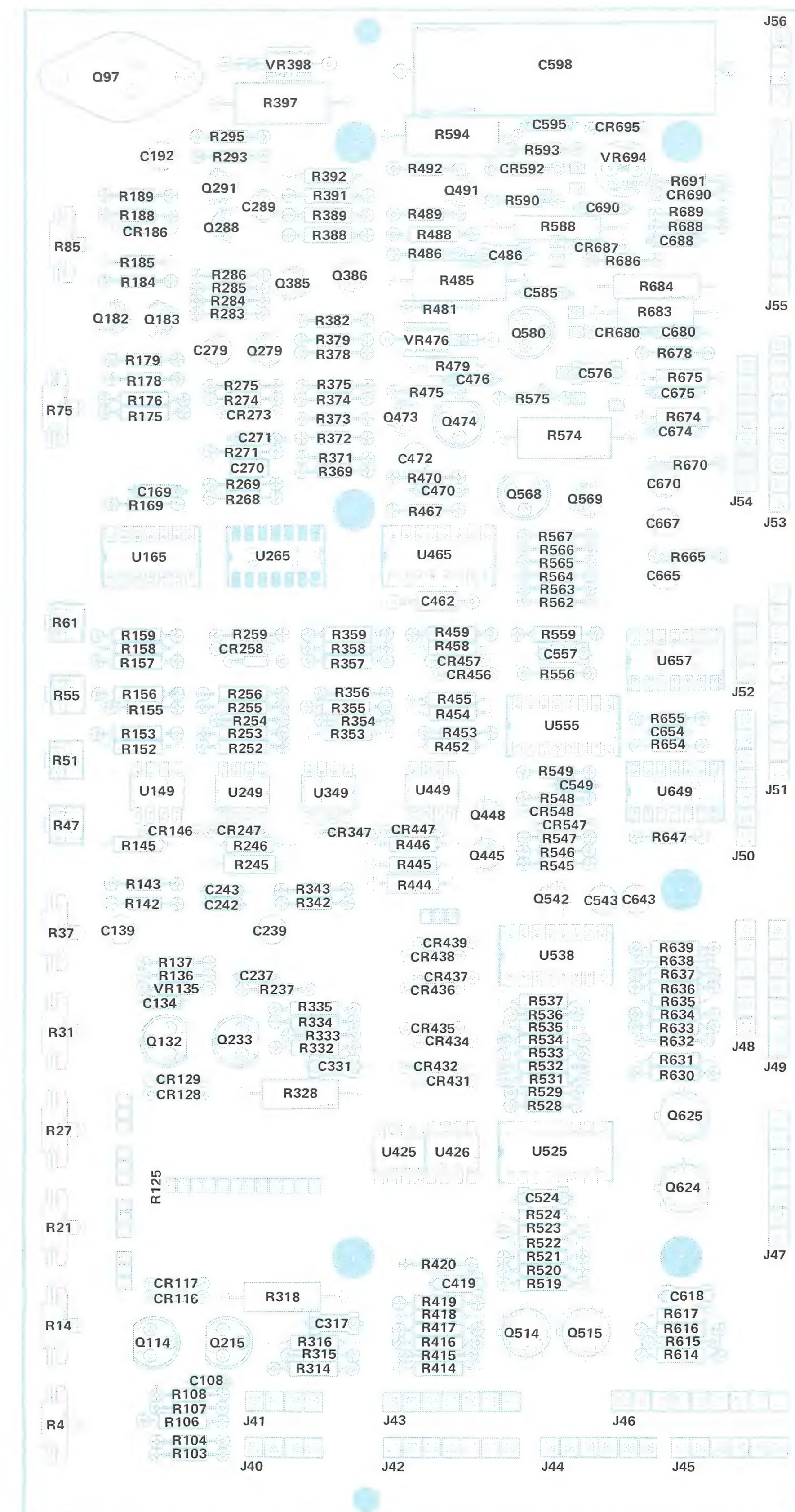
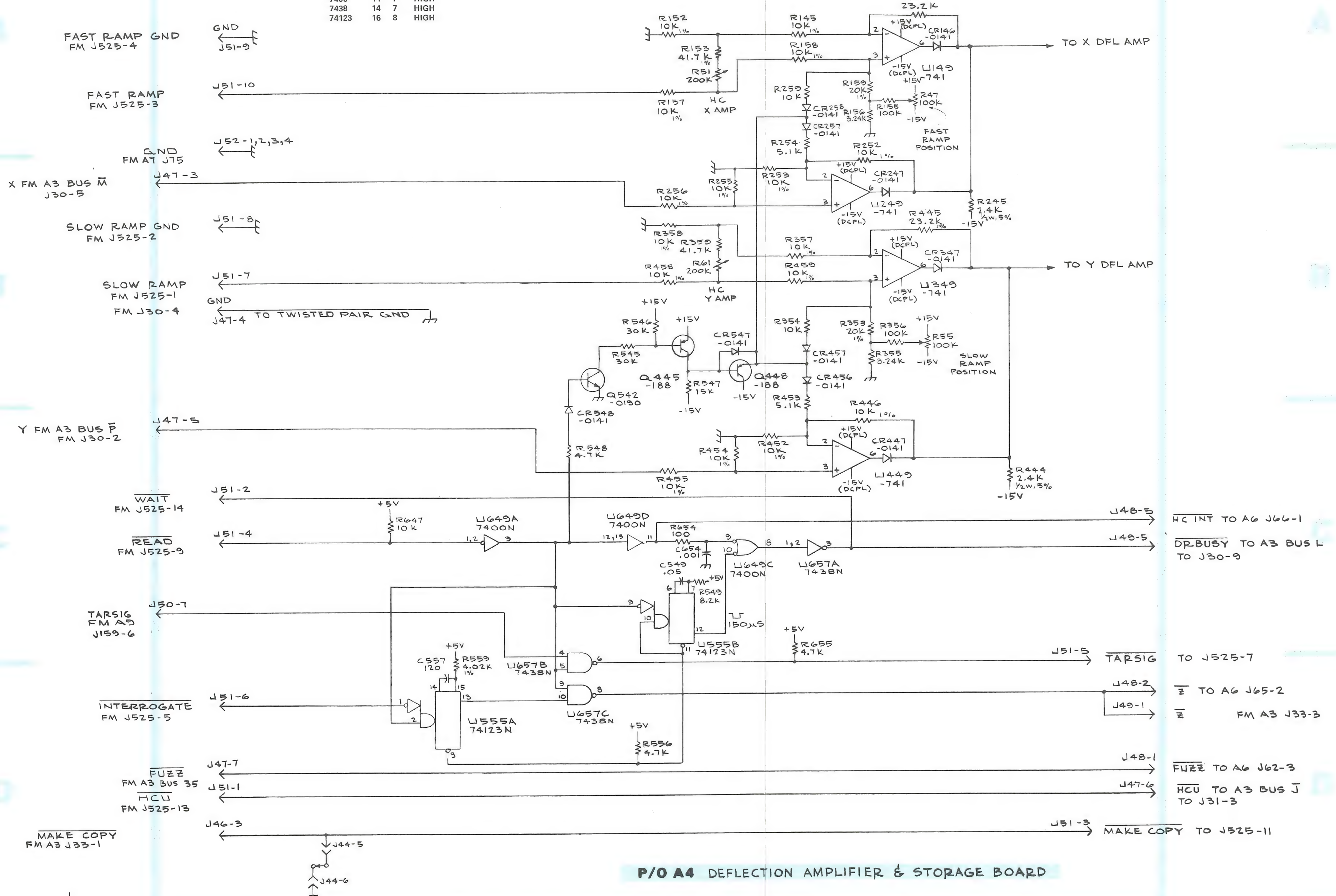


Fig. 6-34B. Deflection Amp and Storage Component Locations. Boards #670-2571-00, 01, 02.

HARD COPY SELECTOR
(BOARD NO.
670-2571-00, 01 & 02)

Semiconductor Information

NUMBER	VCC	GND	UNUSED INPUTS
7400	14	7	HIGH
7438	14	7	HIGH
74123	16	8	HIGH



4012

FIG 6-34A HARD COPY SELECTOR
DAS BOARD # 670-2571-00, 670-2571-01, 670-2571-02

Ⓐ

HARD COPY SELECTOR

CKT NO	GRID LOC
CAPS	
C549	C4
C557	D3
C654	C4
DIODES	
CR146	A5
CR247	B4
CR257	A4
CR258	A4
CR347	B5
CR447	C4
CR456	B4
CR457	B4
CR547	B4
CR548	C3
TRANSISTORS	
Q445	B4
Q448	B4
Q542	B3
RESISTORS	
R47	A5
R51	A4
R55	B5
R61	B4
R145	A4
R152	A4
R153	A4
R155	A4
R156	A4
R157	A4
R158	A4
R159	A4
R245	B5
R246	A5
R252	B4
R253	B4
R254	A4
R255	B4
R256	B4

Ⓐ

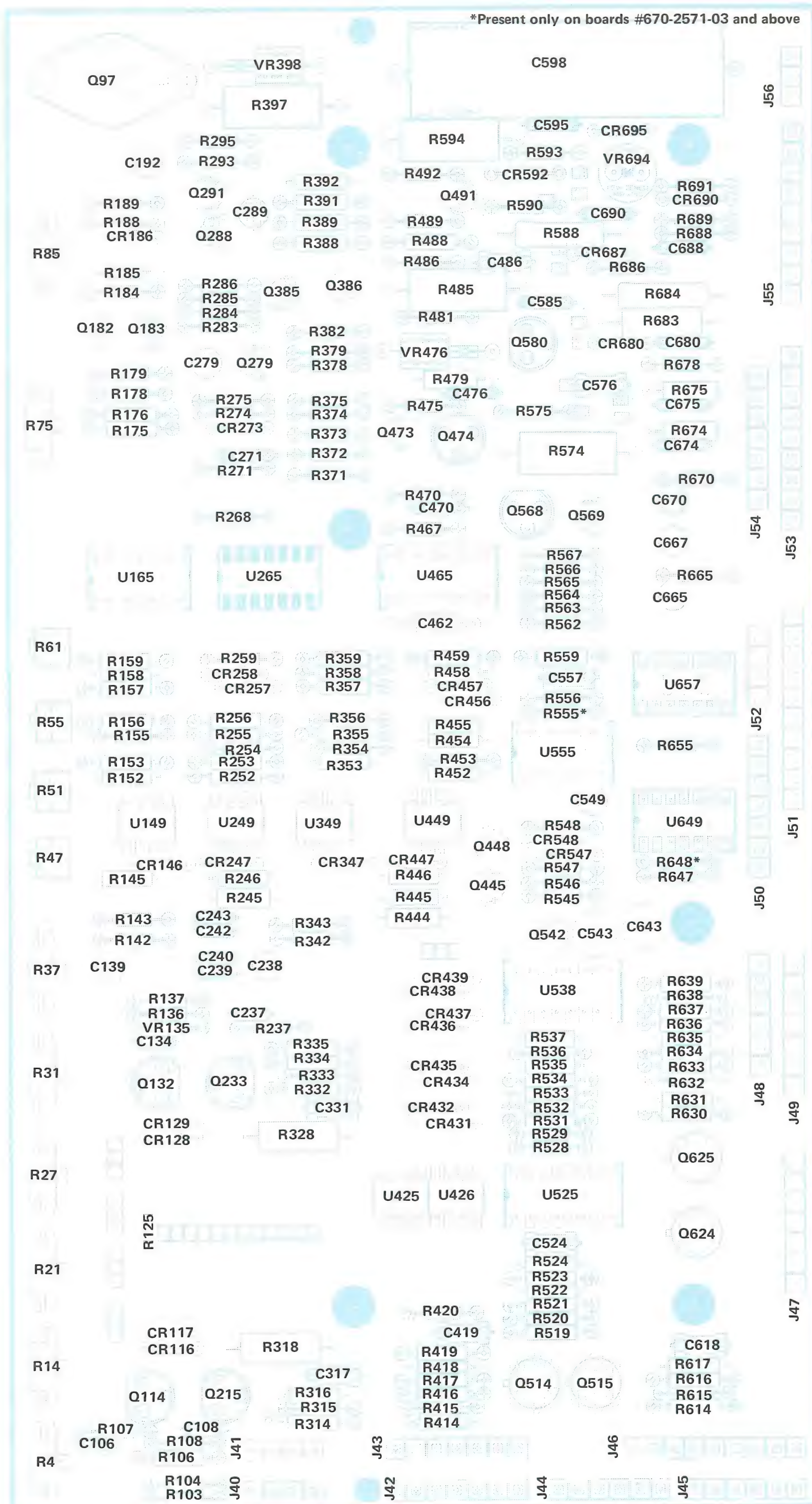


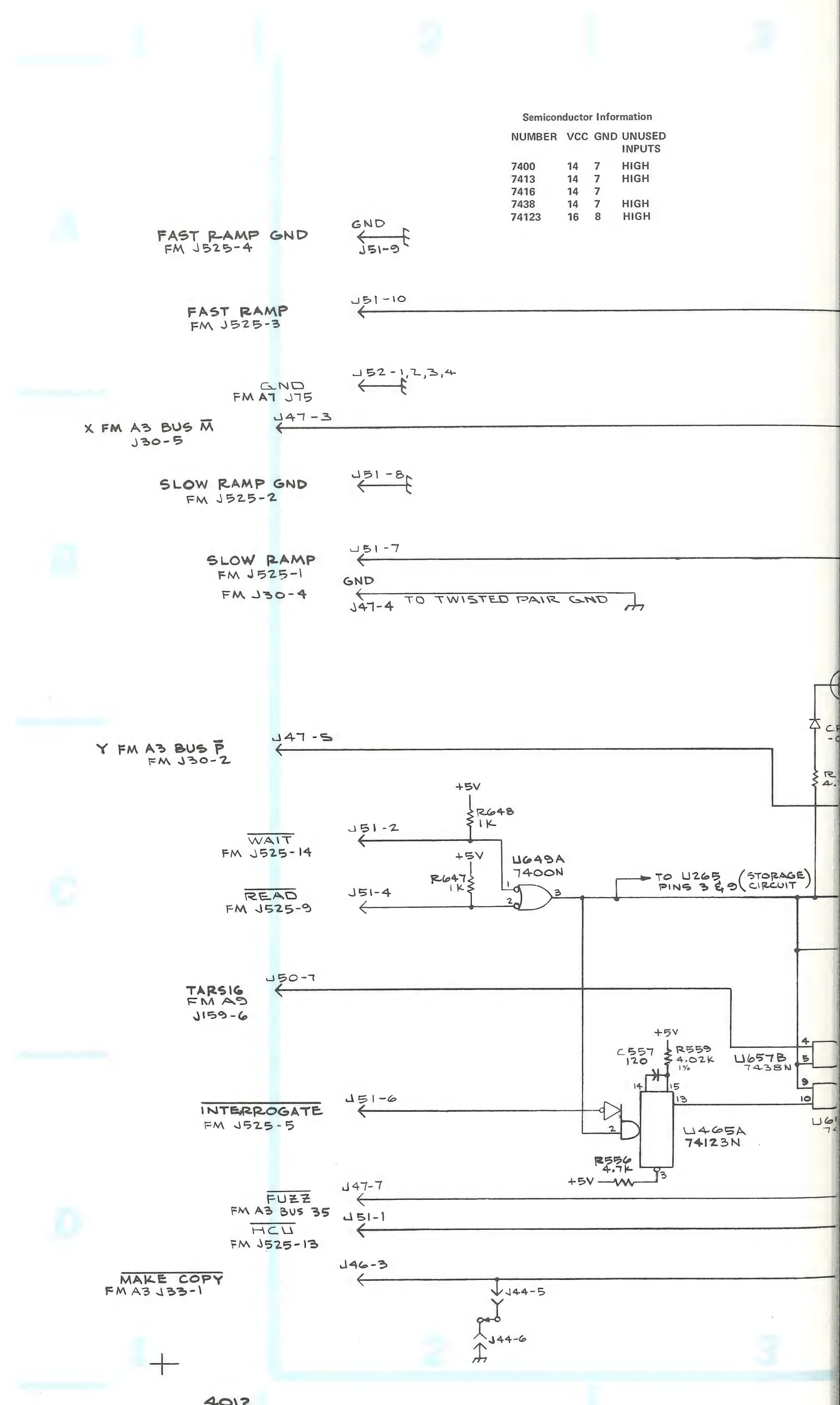
Fig. 6-33. Deflection Amp and Storage Component Locations. Board #670-2571-03.

Ⓐ

HARD COPY SELECTOR

CKT NO	GRID LOC	CKT NO	GRID LOC
CAPS		**RESISTORS**	
C549	C4	R353	B4
C557	D3	R354	B4
		R355	B4
DIODES		R356	B4
		R357	B4
CR146	A5	R358	B4
CR247	B4	R359	B4
CR257	A4	R444	C5
CR258	A4	R445	B5
CR347	B5	R446	C4
CR447	C4	R452	C4
CR456	B4	R453	B4
CR457	B4	R454	C4
CR547	B4	R455	C4
CR548	C3	R458	B4
		R459	B4
TRANSISTORS		R545	B3
		R546	B4
Q445	B4	R547	B4
Q448	B4	R548	C3
Q542	B3	R555	C4
		R556	D3
RESISTORS		R559	D3
		R647	C2
R47	A5	R648	C2
R51	A4	R655	C3
R55	B5		
R61	B4	**IC's**	
R145	A4		
R152	A4	U149	A4
R153	A4	U165E	C3
R155	A4	U165F	C4
R156	A4	U249	B4
R157	A4	U349	B4
R158	A4	U449	C4
R159	A4	U465A	D3
R245	B5	U555A	C4
R246	A5	U555B	C4
R252	B4	U649A	C2
R253	B4	U649D	C3
R254	A4	U657A	C5
R255	B4	U657B	D3
R256	B4	U657C	D3
R259	A4	U657D	C4

Ⓐ



HARD COPY SELECTOR

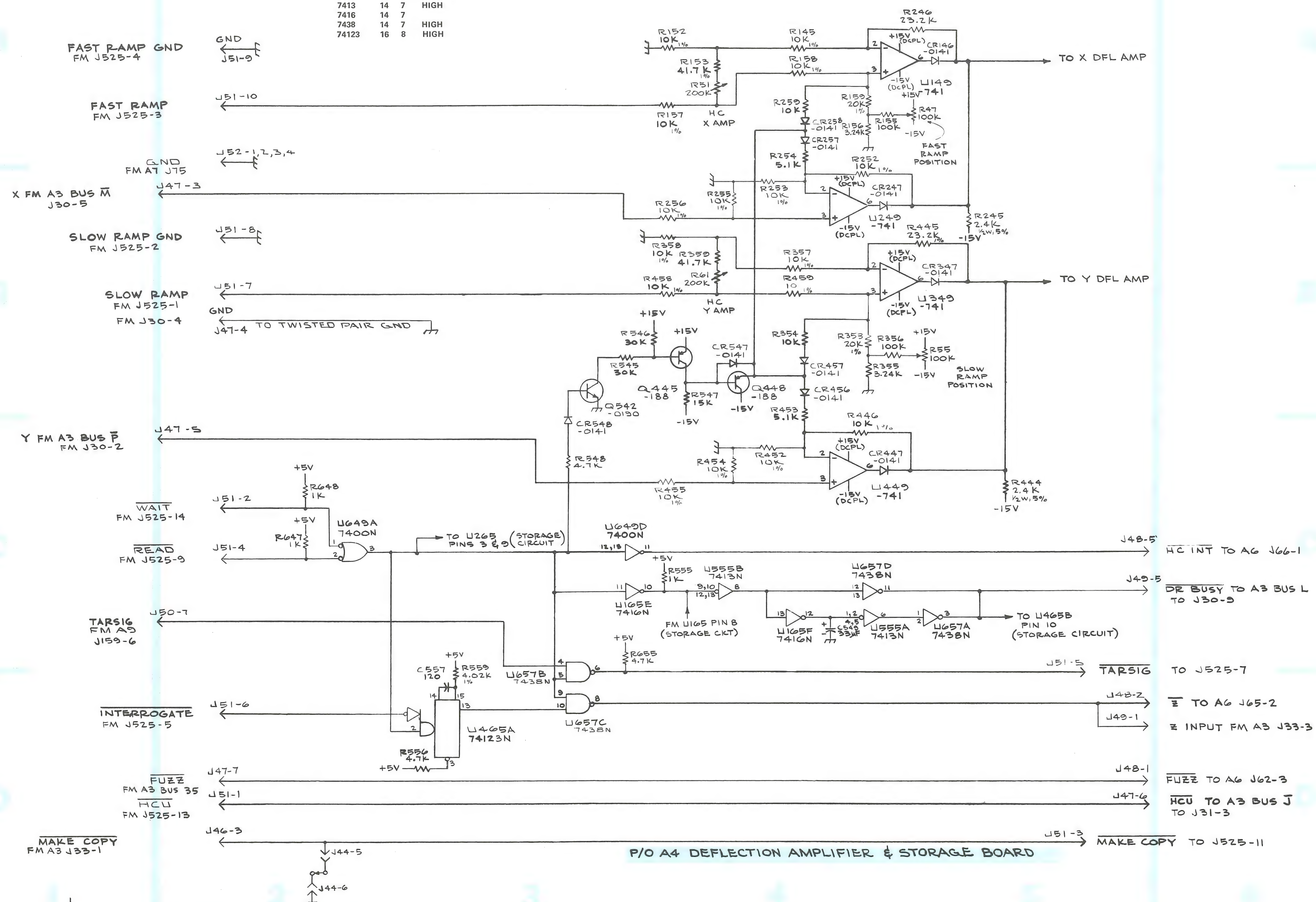
CKT NO	GRID LOC
CAPS	
C549	C4
C557	D3
DIODES	
CR146	A5
CR247	B4
CR257	A4
CR258	A4
CR347	B5
CR447	C4
CR456	B4
CR457	B4
CR547	B4
CR548	C3
TRANSISTORS	
Q445	B4
Q448	B4
Q542	B3
RESISTORS	
R47	A5
R51	A4
R55	B5
R61	B4
R145	A4
R152	A4
R153	A4
R155	A4
R156	A4
R157	A4
R158	A4
R159	A4
R245	B5
R246	A5
R252	B4
R253	B4
R254	A4
R255	B4
R256	B4
R259	A4

CKT NO	GRID LOC
RESISTORS	
R353	B4
R354	B4
R355	B4
R356	B4
R357	B4
R358	B4
R359	B4
R444	C5
R445	B5
R446	C4
R452	C4
R453	B4
R454	C4
R455	C4
R458	B4
R459	B4
R545	B3
R546	B4
R547	B4
R548	C3
R555	C4
R556	D3
R559	D3
R647	C2
R648	C2
R655	C3
IC's	
U149	A4
U165E	C3
U165F	C4
U249	B4
U349	B4
U449	C4
U465A	D3
U555A	C4
U555B	C4
U649A	C2
U649D	C3
U657A	C5
U657B	D3
U657C	D3
U657D	C4

Ⓐ

Semiconductor Information

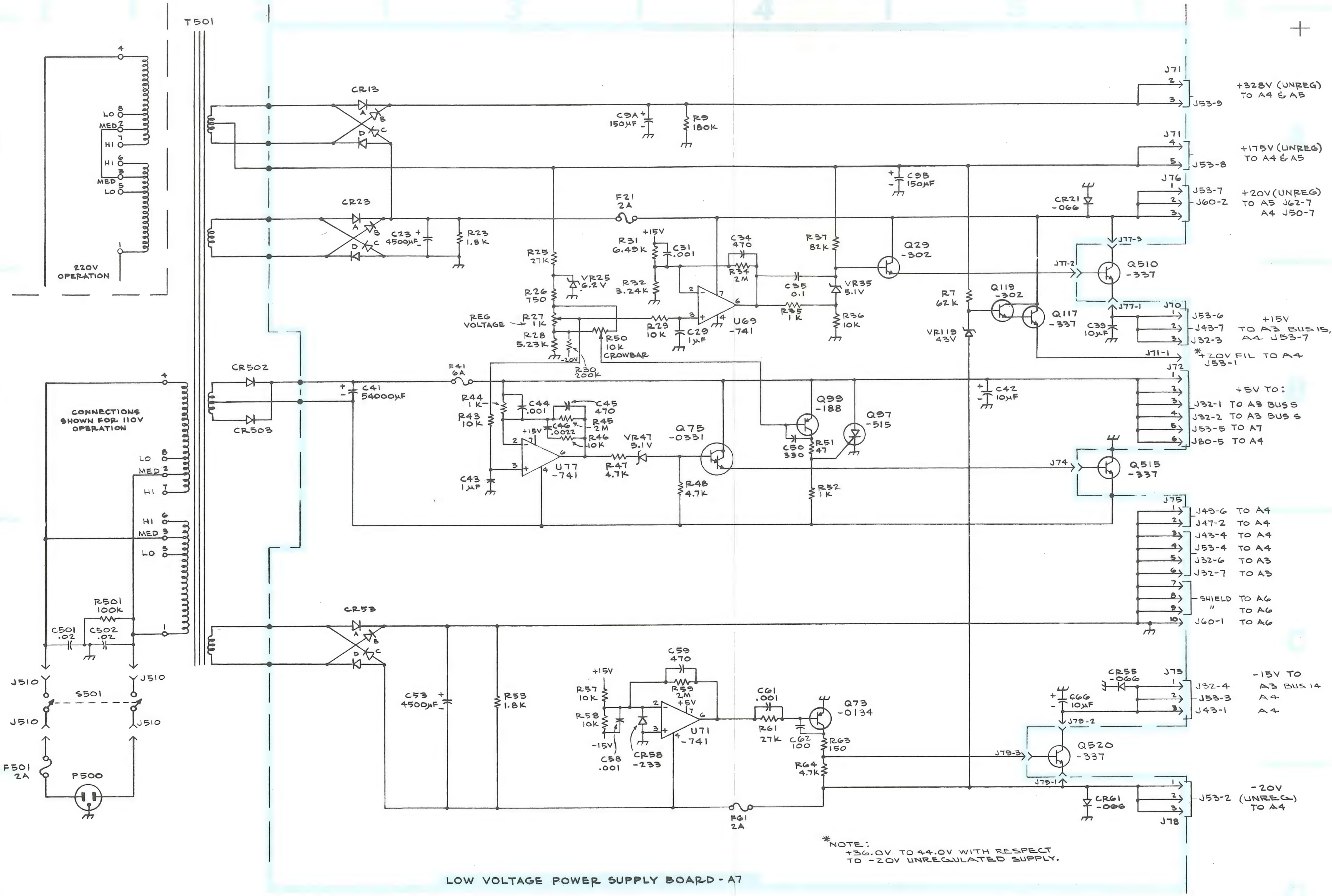
NUMBER	VCC	GND	UNUSED INPUTS
7400	14	7	HIGH
7413	14	7	HIGH
7416	14	7	
7438	14	7	HIGH
74123	16	8	HIGH



Ⓐ

FIG 6-34 HARD COPY SELECTOR
DAS BOARD #670-2571-03

HARD COPY SELECTOR (BOARD NO. 670-2571-03)



4012

FIG 6-37 LV POWER SUPPLY

LV POWER SUPPLY

CKT NO	GRID LOC	CKT NO	GRID LOC
CAPS		TRANSISTORS	
C9A	A3	Q29	A5
C9B	A5	Q73	C4
C23	A3	Q75	B4
C29	B4	Q97	B4
C31	A4	Q99	B4
C34	A4	Q117	B5
C35	B4	Q119	B5
C39	B5	Q510	B5
C41	B2	Q515	B5
C42	B5	Q520	C5
C43	B3		
C44	B3	RESISTORS	
C45	B3		
C46	B3	R7	B5
C50	B4	R9	A4
C53	C3	R23	A3
C58	C3	R25	A3
C59	C4	R26	B3
C61	C4	R27	B3
C62	C4	R28	B3
C66	C5	R29	B4
C501	C1	R30	B3
C502	C1	R31	A4
		R32	B4
		R35	B4
DIODES		R36	B4
		R37	A4
CR13A	A2	R43	B3
CR13B	A2	R44	B3
CR13C	A2	R45	B3
CR13D	A2	R46	B3
CR21	A5	R47	B3
CR23A	A2	R48	B4
CR23B	A2	R50	B3
CR23C	A2	R51	B4
CR23D	A2	R52	B4
CR53A	C2	R53	C3
CR53B	C2	R57	C3
CR53C	C2	R58	C3
CR53D	C2	R59	C4
CR55	C5	R61	C4
CR58	C4	R63	C4
CR61	D5	R64	D4
CR502	B2	R501	C1
CR503	B2		
VR25	B3		
VR35	B4		
VR47	B4	SWITCH	
VR60	D4		
VR119	B5	S501	C1

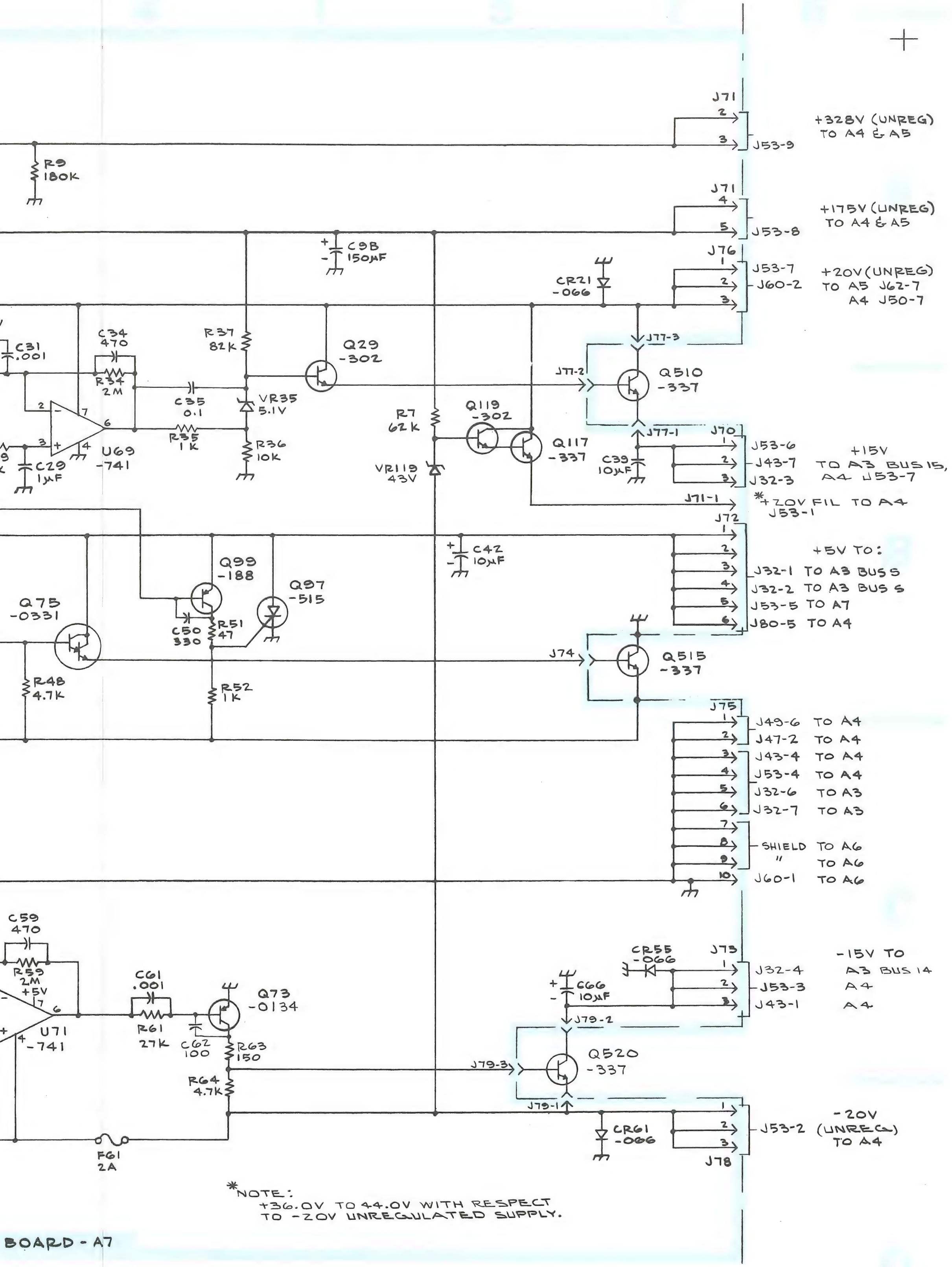


FIG 6-37 LV POWER SUPPLY

Ⓐ

LV POWER SUPPLY

CKT NO	GRID LOC
CAPS	
C9A	A3
C9B	A5
C23	A3
C29	B4
C31	A4
C34	A4
C35	B4
C39	B5
C41	B2
C42	B5
C43	B3
C44	B3
C45	B3
C46	B3
C50	B4
C53	C3
C58	C3
C59	C4
C61	C4
C62	C4
C66	C5
C501	C1
C502	C1
DIODES	
CR13A	A2
CR13B	A2
CR13C	A2
CR13D	A2
CR21	A5
CR23A	A2
CR23B	A2
CR23C	A2
CR23D	A2
CR53A	C2
CR53B	C2
CR53C	C2
CR53D	C2
CR55	C5
CR58	C4
CR61	D5
CR502	B2
CR503	B2
VR25	B3
VR35	B4
VR47	B4
VR60	D4
VR119	B5

CKT NO	GRID LOC
TRANSISTORS	
Q29	A5
Q73	C4
Q75	B4
Q97	B4
Q99	B4
Q117	B5
Q119	B5
Q510	B5
Q515	B5
Q520	C5
RESISTORS	
R7	B5
R9	A4
R23	A3
R25	A3
R26	B3
R27	B3
R28	B3
R29	B4
R30	B3
R31	A4
R32	B4
R35	B4
R36	B4
R37	A4
R43	B3
R44	B3
R45	B3
R46	B3
R47	B3
R48	B4
R50	B3
R51	B4
R52	B4
R53	C3
R57	C3
R58	C3
R59	C4
R61	C4
R63	C4
R64	D4
R501	C1
SWITCH	
S501	C1

CKT NO	GRID LOC
IC's	
U69	B4
U71	C4
U77	B3
FUSES	
F21	A3
F41	B3
F61	D4
F501	C1
TRANSFORMERS	
T501	A2
	B2
	C2

Ⓐ

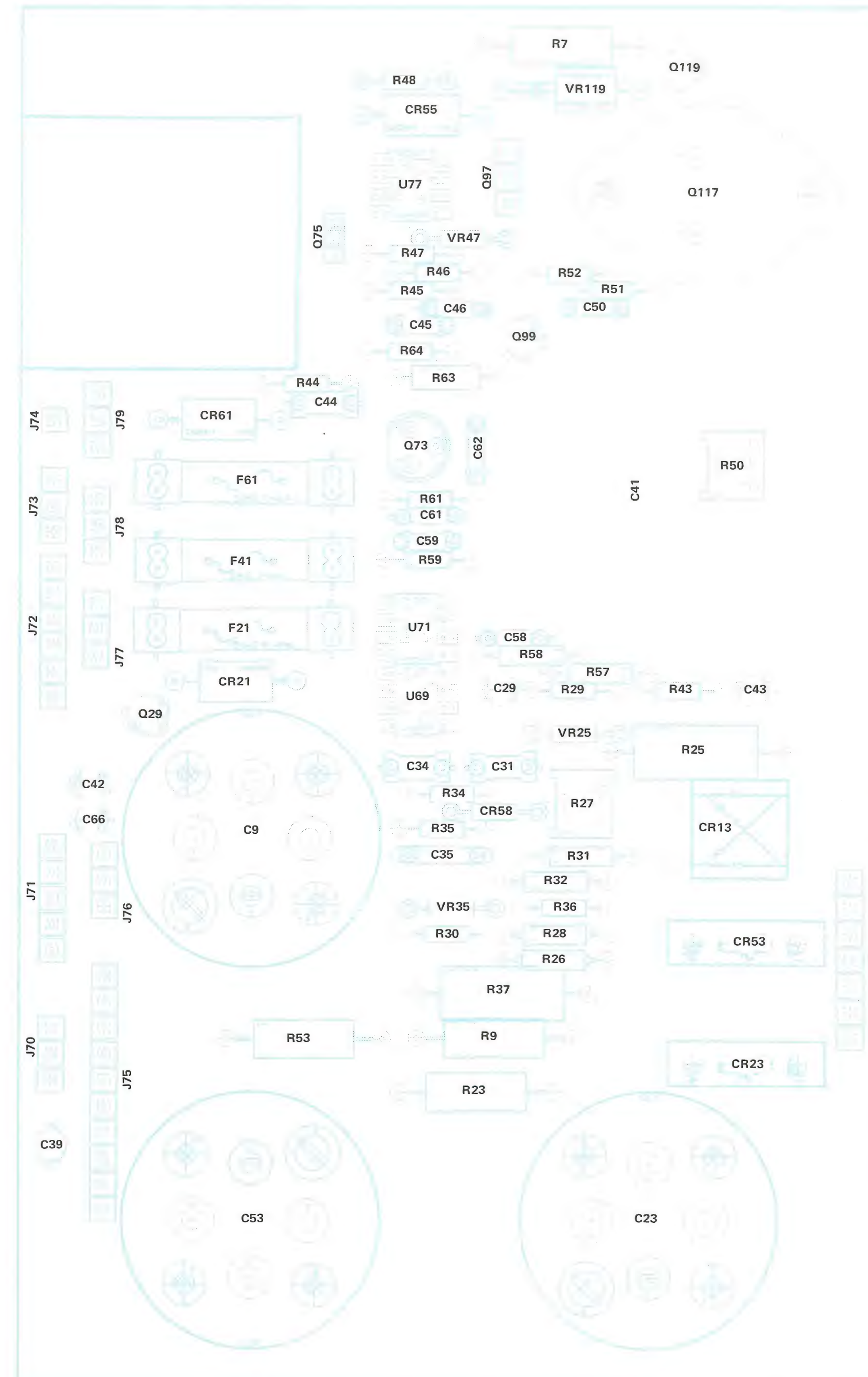


Fig. 6-38. Low Voltage Power Supply Component Locations.

Ⓐ

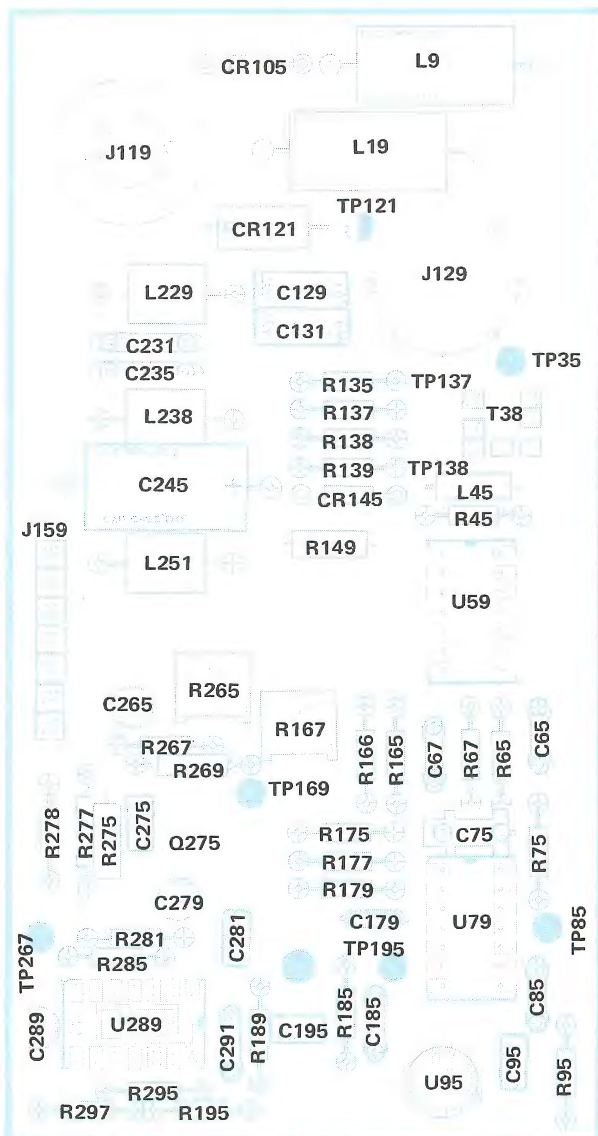


Fig. 6-35. Hard Copy Tarsig Amplifier Component Locations.

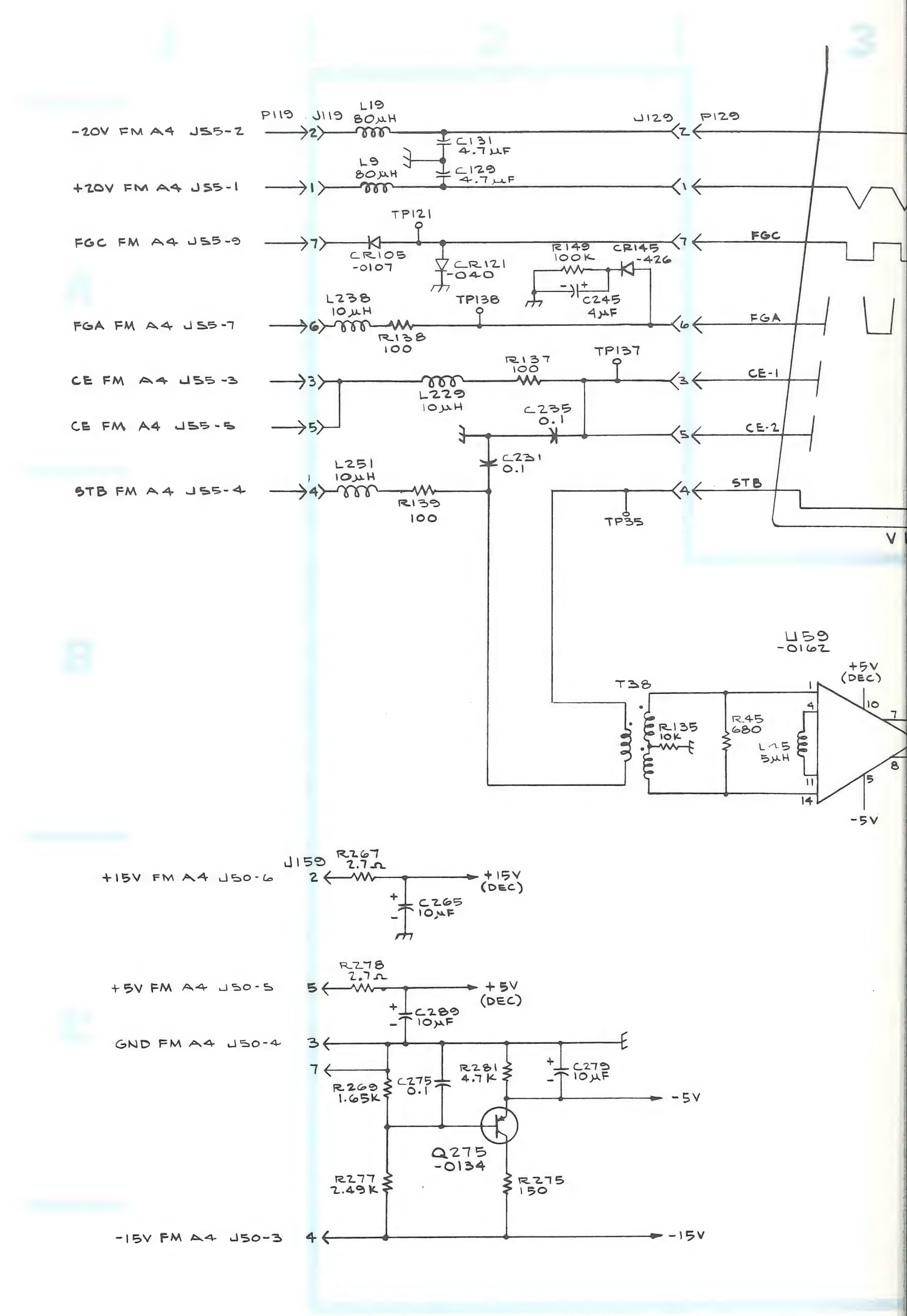
Ⓐ

HARD COPY TARSIG AMPLIFIER

CKT NO	GRID LOC
CAPS	
C65	B3
C67	B3
C75	B3
C85	B4
C95	B4
C129	A2
C131	A2
C179	C4
C185	B4
C195	B5
C231	A2
C235	A2
C245	A2
C265	C2
C275	C2
C279	C2
C281	B4
C289	C2
C291	B5
DIODES	
CR105	A2
CR121	A2
CR145	A2
INDUCTORS	
L9	A2
L19	A2
L45	B3
L229	A2
L238	A2
L251	B2
TRANSISTORS	
Q275	C2

CKT NO	GRID LOC
RESISTORS	
R45	B3
R65	B3
R67	B3
R75	B4
R95	B4
R135	B2
R137	A2
R138	A2
R139	B2
R149	A2
R165	B3
R166	B3
R167	C4
R175	C5
R177	C4
R179	C4
R185	B4
R189	C4
R195	B5
R265	C5
R267	C2
R269	C2
R275	C2
R277	C2
R278	C2
R281	C2
R285	B5
R295	B5
R297	B5
IC's	
U59	B3
U79	B4
U95	B4
U289	B5
XFMR	
T38	B2

Ⓐ



Semiconductor Information

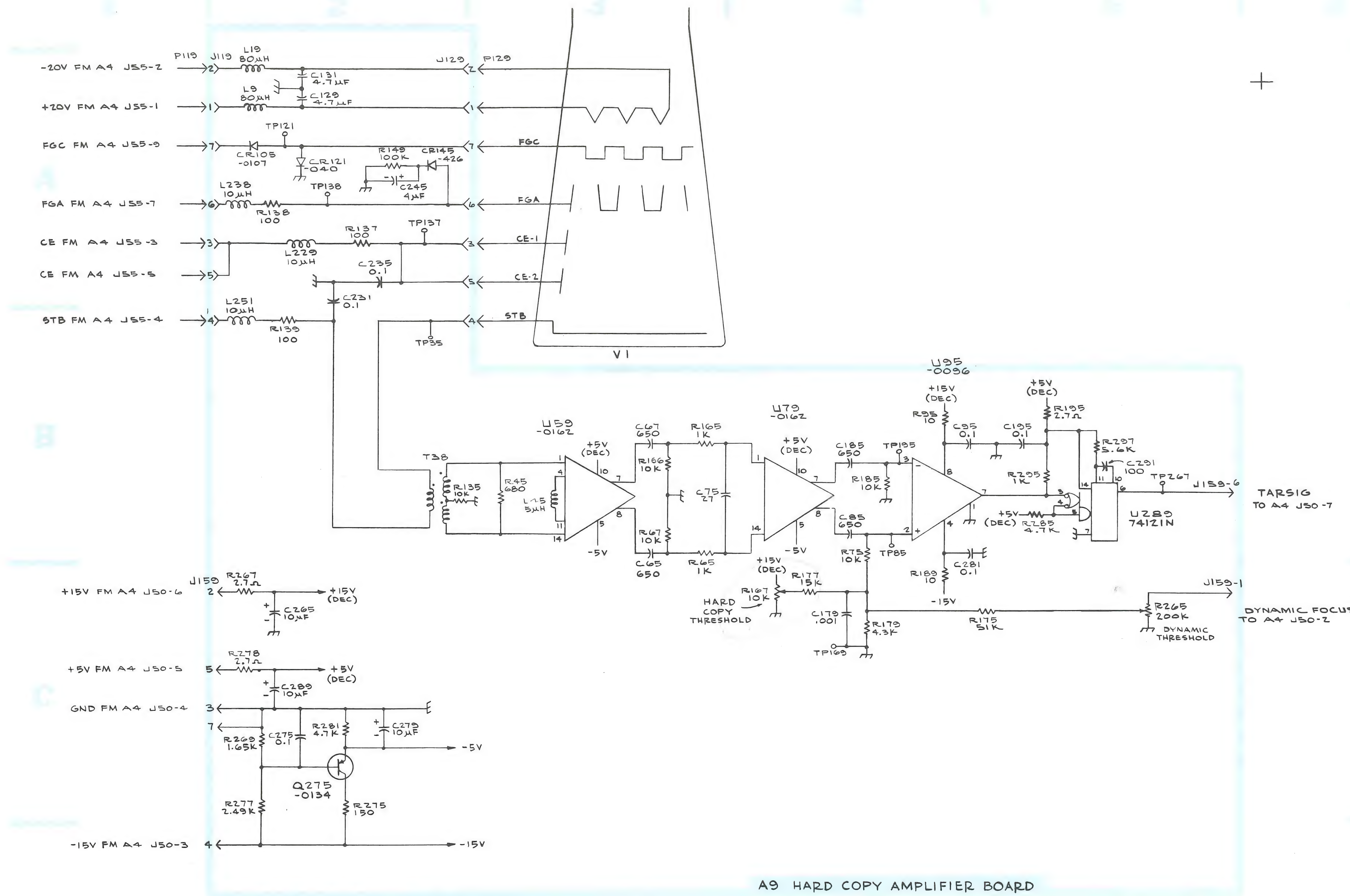
NUMBER	VCC	GND	UNUSED INPUTS
74121	14	7	HIGH

4012

D COPY TARSIG AMPLIFIER

	GRID LOC	CKT NO	GRID LOC
S		RESISTORS	
	B3	R45	B3
	B3	R65	B3
	B3	R67	B3
	B4	R75	B4
	B4	R95	B4
	A2	R135	B2
	A2	R137	A2
	C4	R138	A2
	B4	R139	B2
	B5	R149	A2
	A2	R165	B3
	A2	R166	B3
	A2	R167	C4
	C2	R175	C5
	C2	R177	C4
	C2	R179	C4
	B4	R185	B4
	C2	R189	C4
	B5	R195	B5
		R265	C5
		R267	C2
DES		R269	C2
		R275	C2
05	A2	R277	C2
21	A2	R278	C2
35	A2	R281	C2
		R285	B5
		R295	B5
UCTORS		R297	B5
	A2	IC's	
	A2		
	B3	U59	B3
	A2	U79	B4
	A2	U95	B4
	B2	U289	B5
NSISTORS		XFMR	
	C2	T38	B2

Ⓐ



Semiconductor Information

NUMBER	VCC	GND	UNUSED INPUTS
74121	14	7	HIGH

3-133

4012 Ⓐ FIG 6-36

HARD COPY TARSIG AMPLIFIER

AMPLIFIER

LOW-VOLTAGE POWER SUPPLY

Refer to the Low-Voltage Power Supply schematic, Fig. 6-37. This power supply has regulated outputs of −15 volts, +5 volts, and +15 volts. It also has unregulated outputs of −20 volts, +20 volts, +175 volts, and +328 volts.

Unregulated Supplies. All of these, except for +175 volts, obtain their power from conventional, full-wave bridge rectifier circuits. The +175 volt supply uses a full-wave center-tapped transformer configuration. The sources for the +328 volts, +175 volts, and +20 volts are connected in series-aiding, with each supply being referenced to the next lower supply. For example, two windings are in series to provide power for the +328 volt circuit.

Three fuses provide protection for the power supply circuits. F21 fuses the +15 volt and +20 volt supplies. F41 fuses the +5 volt supply and F61 fuses the −20 volt and −15 volt supplies.

Regulated Supplies. VR25 develops the 6.2 volts that is used as reference for the +15 volt and +5 volt supplies. A portion of this is picked off by R27 and is applied as reference to the positive inputs of U69 and U77. The regulated +15 volt output is applied through a voltage divider to the negative input of U69 to provide regulating drive to that amplifier. Outputs from U69 are applied through VR35 to Q29 to control the drive current to series regulator Q510.

The regulated +5 volts is applied through R44 to the negative input of U77. U77 compares this against the voltage at the positive input to generate a regulating output voltage, which is applied to Q75 to control the drive current to series regulator Q515. Q99 and Q97 provide the +5 volt circuits with over-voltage protection. Under normal conditions, the +5 volts applied to the emitter of Q99 is insufficient to cause the device to conduct, since its base is held at approximately 4.8 volts by R50. If the +5 volt line should go as high as 5.4 volts, Q99 conducts. When the voltage at the gate of Q97 reaches 1.2 volts, Q97 conducts and immediately lowers the +5 volt line to approximately 1 volt. The associated surge of current causes F41 to open up, removing power from the circuit.

The −15 Volt regulator uses ground for a reference at the input of U71. The negative input receives its signal from a comparison between the +15 volt supply and the −15 volt supply applied through voltage divider R57 and R58. Any deviations on the −15 volt line cause drive to U71, which provides a signal to the error amplifier Q73. This controls the drive to Q520, regulating the −15 volt supply.

MECHANICAL PARTS LIST

Replacement parts should be ordered from the Tektronix Field Office or Representative in your area. Changes to Tektronix products give you the benefit of improved circuits and components. Please include the instrument type number and serial number with each order for parts or service.

ABBREVIATIONS

BHB	binding head brass	h	height or high	OHB	oval head brass
BHS	binding head steel	hex.	hexagonal	OHS	oval head steel
CRT	cathode-ray tube	HHB	hex head brass	PHB	pan head brass
csk	countersunk	HHS	hex head steel	PHS	pan head steel
DE	double end	HSB	hex socket brass	RHS	round head steel
FHB	flat head brass	HSS	hex socket steel	SE	single end
FHS	flat head steel	ID	inside diameter	THB	truss head brass
Fil HB	fillister head brass	lg	length or long	THS	truss head steel
Fil HS	fillister head steel	OD	outside diameter	w	wide or width

FIGURE 1 KEYBOARD & CABINET

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Qty	Description 1 2 3 4 5
1-1	386-2415-00			1	PANEL,KEYBOARD
					(ATTACHING PARTS)
-2	211-0507-00			6	SCREW,6-32 X 0.372 INCH,PHS
-3	211-0006-00			4	WASHER,LOCK,INTERNAL,0.146 ID X 0.286 INCH OD
					- - - * - - -
-4	119-0374-00			1	KEYBOARD ASSEMBLY, 60 KEY, A8
	- - - - - -			-	KEYBOARD ASSEMBLY INCLUDES:
-5	- - - - - -			60	CAP (ORDER BY DESCRIPTION)
-6	119-0447-00			1	SPACER BAR ASSEMBLY
					(ATTACHING PARTS)
-7	211-0517-00			6	SCREW,6-32 X 0.50 INCH,PHS
					- - - * - - -
-8	136-0148-00			1	SOCKET, 15 PIN
-9	214-0702-00			1	KEY,POLARIZING,CONNECTOR
-10	343-0003-00			1	CLAMP,PLASTIC,CABLE,0.25 INCH
					(ATTACHING PARTS)
-11	211-0014-00			1	SCREW,4-40 X 0.50 INCH,PHS
	210-0851-00			1	WASHER,FLAT,0.119 ID X 0.375 INCH OD (NOT SHOWN)
-12	210-0586-00			1	NUT,KEPS,4-40 X 0.25 INCH
					- - - * - - -
-13	366-0128-01			2	KNOB,THUMBWHEEL
	- - - - - -			-	EACH KNOB INCLUDES:
	213-0076-00			2	SETSCREW,2-56 X 0.125 INCH,HSS
-14	407-0994-00			1	BRACKET,ANGLE
					(ATTACHING PARTS)
-15	210-0586-00			2	NUT,KEPS,4-40 X 0.25 INCH
					- - - * - - -
-16	- - - - - -			2	RESISTOR,VARIABLE
					(ATTACHING PARTS FOR EACH)
-17	210-0583-00			2	NUT,HEX.,0.25-32 X 0.312 INCH
-18	210-0046-00			1	WASHER,LOCK,INTERNAL,0.261 ID X 0.40 INCH OD
					- - - * - - -

FIGURE 1 KEYBOARD & CABINET (cont)

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Qty	Description 1 2 3 4 5
1-19	- - - - - -			1	LAMP,W/GREEN LENS
-20	- - - - - -			2	LIGHT EMITTING DIODE,W/MOUNTING CLIP
-21	131-0775-00			1	TERMINAL,STUD,HEX.
-22	260-1334-00			4	SWITCH,ROCKER
					(ATTACHING PARTS FOR EACH)
-23	210-0406-00			2	NUT,HEX.,4-40 X 0.188 INCH
-24	210-0004-00			2	WASHER,LOCK,INTERNAL,0.12 ID X 0.26 INCH OD
-25	166-0024-00			2	TUBE,SPACER,0.125 INCH LONG
					- - - * - - -
-26	390-0310-00			1	CABINET TOP,DISPLAY UNIT
					(ATTACHING PARTS)
-27	211-0540-00			3	SCREW,6-32 X 0.50 INCH,THS
					- - - * - - -
-28	200-1290-01			2	COVER,SIDE,RIGHT & LEFT
					(ATTACHING PARTS FOR EACH)
-29	211-0540-00			2	SCREW,6-32 X 0.50 INCH,THS
					- - - * - - -
-30	437-0144-00			1	CABINET,DISPLAY UNIT
					(ATTACHING PARTS)
-31	212-0507-00			4	SCREW,10-32 X 0.375 INCH,PHS
					- - - * - - -
-32	348-0015-00			4	CUSHION,RUBBER BALL
-33	348-0014-00			4	FOOT,BLACK PLASTIC
					(ATTACHING PARTS FOR EACH)
-34	211-0513-00			1	SCREW,6-32 X 0.625 INCH,PHS
					- - - * - - -
-35	119-0305-00			1	SPEAKER
					(ATTACHING PARTS)
-36	210-0457-00			4	NUT,KEPS,6-32 X 0.312 INCH
					- - - * - - -
-37	- - - - - -			1	RESISTOR,VARIABLE
					(ATTACHING PARTS)
-38	210-0583-00			1	NUT,HEX.,0.25-32 X 0.312 INCH
					- - - * - - -
-39	366-0261-00			1	KNOB,GRAY,PLASTIC
	- - - - - -			-	KNOB INCLUDES:
	214-0395-00			1	SPRING,WIRE (NOT SHOWN)
-40	- - - - - -			-	RESISTOR,VARIABLE
					(ATTACHING PARTS)
	213-0020-00			1	SETSCREW,6-32 X 0.125 INCH,HSS (NOT SHOWN)
					- - - * - - -
-41	255-0334-00			IN	PLASTIC CHANNEL,4.875 INCHES LONG
-42	343-0015-00			1	CLAMP,CABLE,STAINLESS STEEL,0.50 INCH
					(ATTACHING PARTS)
-43	210-0457-00			1	NUT,KEPS,6-32 X 0.312 INCH
-44	210-0202-00			1	TERMINAL,LUG,SOLDER,SE #6
					- - - * - - -

FIGURE 1 KEYBOARD & CABINET (cont)

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Serial/Model No. Disc	Qty	1 2 3 4 5 Description
1-45	386-2432-00			1	PANEL,REAR
					(ATTACHING PARTS)
-46	211-0507-00			6	SCREW,6-32 X 0.312 INCH,PHS
-47	210-0006-00			6	WASHER,LOCK,INTERNAL,0.146 ID X 0.283 INCH OD
					- - - * - - -
-48	337-1518-00			1	SHIELD,H.V.
					(ATTACHING PARTS)
-49	211-0097-00			3	SCREW,4-40 X 0.312 INCH,PHS
					- - - * - - -
-50	- - - - - -			1	CIRCUIT BOARD ASSY--HIGH VOLTAGE & Z AXIS A6
	- - - - - -			-	CIRCUIT BOARD ASSEMBLY INCLUDES:
-51	131-0589-00			22	TERMINAL,PIN,0.46 INCH LONG
-52	214-0579-00			1	PIN,TEST POINT
-53	214-1292-00			2	HEATSINK
-54	- - - - - -			1	RESISTOR,VARIABLE
					(ATTACHING PARTS)
-55	210-0413-00			1	NUT,HEX.,0.375-32 X 0.50 INCH
-56	210-0840-00			1	WASHER,FLAT,0.39 ID X 0.562 INCH OD
-57	210-0012-00			1	WASHER,LOCK,INTERNAL,0.375 ID X 0.50 INCH OD
					- - - * - - -
-58	376-0011-00			1	COUPLING,PLASTIC
	- - - - - -			-	COUPLING INCLUDES:
	213-0048-00			2	SETSCREW,4-40 X 0.125 INCH,HSS
-59	385-0120-00			1	ROD,PLASTIC
-60	129-0178-00			2	POST,PLASTIC,1.37 INCHES LONG
					(ATTACHING PARTS FOR EACH)
-61	211-0040-00			1	SCREW,4-40 X 0.25 INCH,PLASTIC,BS
					- - - * - - -
-62	385-0075-00			1	INSULATOR,STANDOFF
					(ATTACHING PARTS)
-63	211-0558-00			1	SCREW,6-32 X 0.25 INCH,PLASTIC,BS
					- - - * - - -
-64	384-0616-00			1	ROD,SPACER,1.37 INCHES LONG
					(ATTACHING PARTS)
-65	211-0097-00			1	SCREW,4-40 X 0.312 INCH,PHS
					- - - * - - -
	131-1334-00			1	LINK,TERMINAL CONNECTOR (NOT SHOWN)
	- - - - - -			-	LINK INCLUDES:
	131-0621-00			2	CONNECTOR,TERMINAL
	352-0198-00			1	HOLDER,TERMINAL CONNECTOR,2 WIRE
-66	- - - - - -			1	TRANSISTOR
					(ATTACHING PARTS)
-67	211-0511-00			2	SCREW,6-32 X 0.50 INCH,PHS
					- - - * - - -
-68	214-1610-00			1	HEATSINK
-69	407-0993-00			1	BRACKET
-70	166-0203-00			1	TUBE,SPACER,PLASTIC,0.062 INCH LONG
-71	136-0361-00			1	SOCKET,TRANSISTOR
-72	131-0847-00			2	TERMINAL POST
-73	136-0384-00			2	SOCKET,PIN TERMINAL

FIGURE 1 KEYBOARD & CABINET (cont)

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Serial/Model No. Disc	Qty	Description 1 2 3 4 5
1-74	136-0486-00			1	ASSEMBLY,CRT SOCKET
	- - - - - - -			-	ASSEMBLY INCLUDES:
	136-0278-00			1	SOCKET,CRT
	- - - - - - -			-	SOCKET INCLUDES:
	204-0322-00			1	BODY,CRT SOCKET
	214-0464-00			7	CONTACT,CRT SOCKET
					(ATTACHING PARTS)
-75	211-0116-00			5	SCREW,SEMS,4-40 X 0.312 INCH,PHB
-76	210-0586-00			2	NUT,KEPS,4-40 X 0.25 INCH
	129-0080-00			1	POST,PLASTIC,0.875 INCH LONG (NOT SHOWN)
	211-0040-00			1	SCREW,4-40 X 0.25 INCH,BH (NOT SHOWN)
					- - - * - - -
-77	179-1950-01			-	WIRING HARNESS,HARD COPY
	- - - - - - -			-	WIRING HARNESS INCLUDES:
-78	131-0621-00			27	CONNECTOR,TERMINAL
	131-0622-00			6	CONNECTOR,TERMINAL
	131-0792-00			6	CONNECTOR,TERMINAL
-79	352-0198-00			1	HOLDER,TERMINAL CONNECTOR,2 WIRE
-80	352-0200-00			1	HOLDER,TERMINAL CONNECTOR,4 WIRE
-81	352-0203-00			2	HOLDER,TERMINAL CONNECTOR,7 WIRE
-82	352-0205-00			1	HOLDER,TERMINAL CONNECTOR,9 WIRE
-83	352-0206-00			1	HOLDER,TERMINAL CONNECTOR,10 WIRE
-84	136-0271-00			1	SOCKET,TUBE,7 PIN
-85	131-1187-00			1	CONNECTOR COVER
-86	131-0458-00			1	CONNECTOR,15 PIN, FEMALE
					(ATTACHING PARTS)
-87	129-0260-00			2	POST,METALLIC,STUD
-88	210-0201-00			1	TERMINAL,LUG,SOLDER
-89	210-0003-00			1	WASHER,LOCK,EXTERNAL,0.12 ID X 0.25 INCH OD
-90	210-0406-00			2	NUT,HEX.,4-40 X 0.188 INCH
					- - - * - - -
	131-0621-00			6	CONNECTOR,TERMINAL
-91	352-0202-00			1	HOLDER,TERMINAL CONNECTOR,6 WIRE
-92	175-0859-00			FT	WIRE,ELECTRICAL,6 WIRE RIBBON,0.833 FT(TOTAL)
	179-1951-00			1	WIRING HARNESS,KEYBOARD
	- - - - - - -			-	WIRING HARNESS INCLUDES:
-93	131-0707-00			4	CONNECTOR,TERMINAL
	131-0621-00			14	CONNECTOR,TERMINAL
-94	352-0169-00			2	HOLDER,TERMINAL CONNECTOR,2 WIRE
	352-0200-00			1	HOLDER,TERMINAL CONNECTOR,4 WIRE
	352-0202-00			1	HOLDER,TERMINAL CONNECTOR,6 WIRE
	352-0203-00			1	HOLDER,TERMINAL CONNECTOR,7 WIRE

FIG. 1 KEYBOARD & CABINET

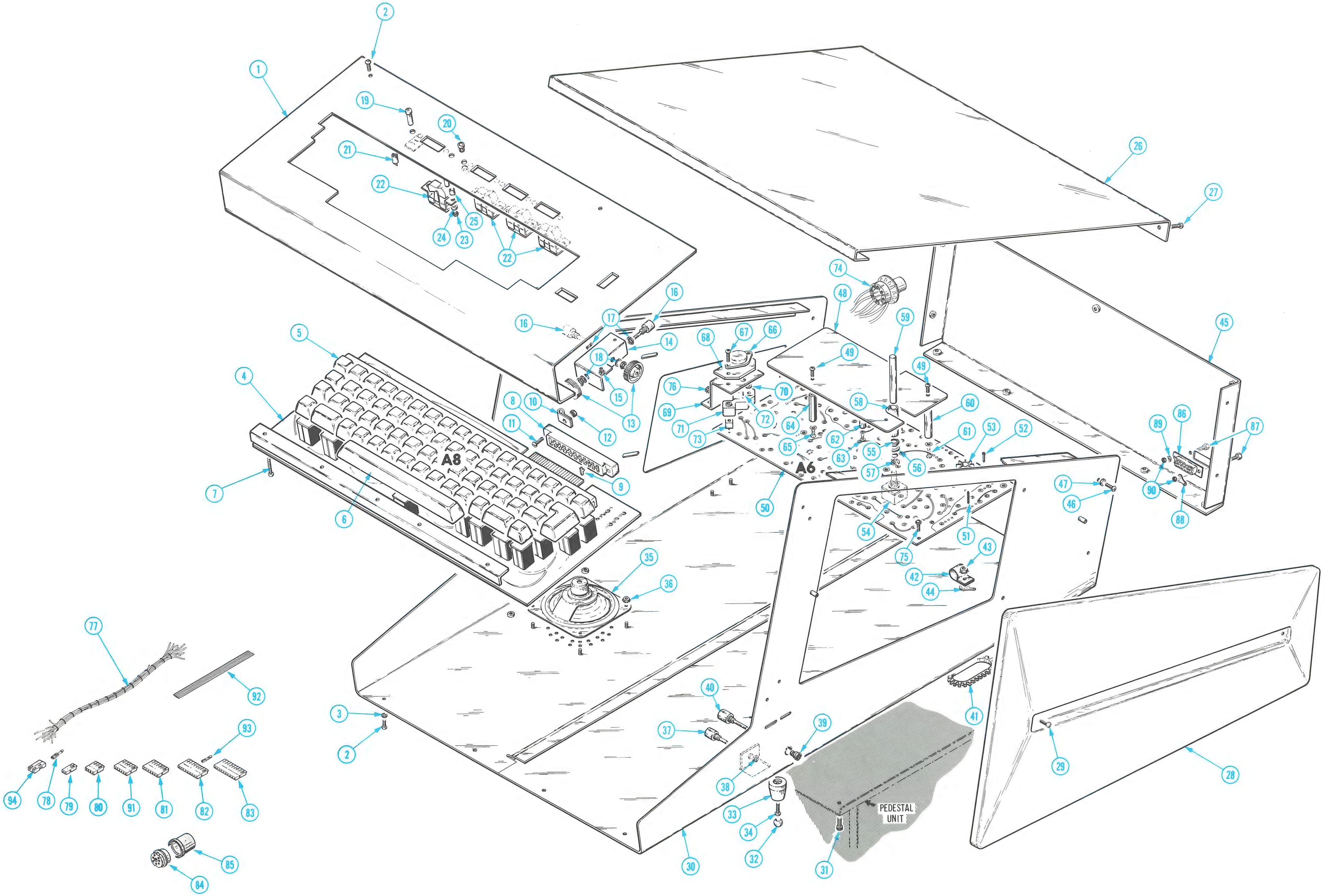
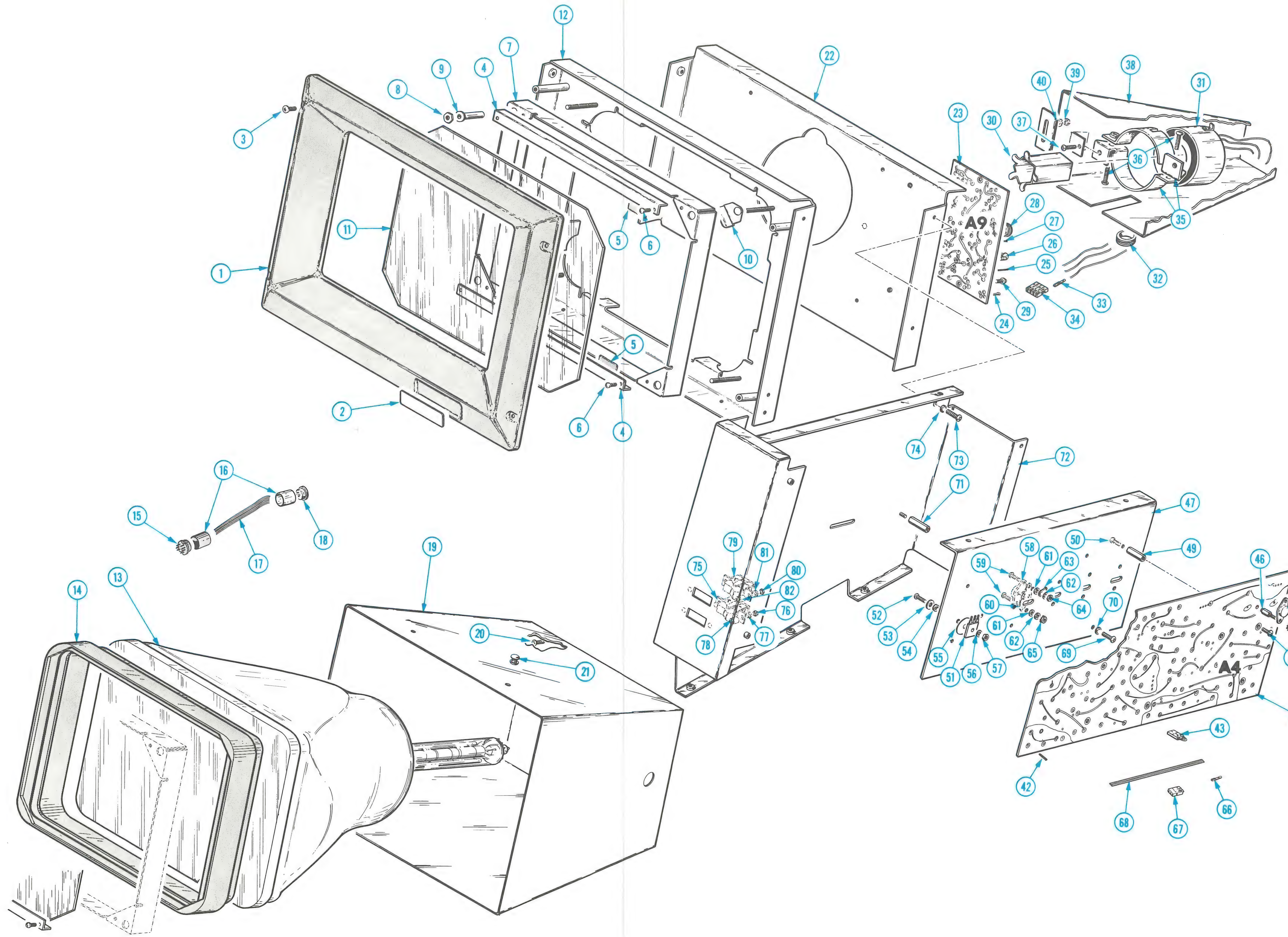


FIG. 2 PROC...



Ⓐ

FIGURE 2 FRONT & CRT

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Qty	Description 1 2 3 4 5
2-1	331-0299-05			1	MASK,GRATICULE
	- - - - - - -			-	MASK INCLUDES:
-2	334-1844-04			1	PLATE,IDENTIFICATION
					(ATTACHING PARTS)
-3	211-0581-00			4	SCREW,6-32 X 0.375 INCH,THS
					- - - * - - -
-4	407-0997-00			2	BRACKET,ANGLE
	- - - - - - -			-	EACH BRACKET INCLUDES:
-5	124-0050-00			1	STRIP,PLASTIC,FOAM,9.875 INCHES LONG
					(ATTACHING PARTS FOR EACH)
-6	211-0065-00			2	SCREW,4-40 X 0.188 INCH,PHS
					- - - * - - -
-7	426-0834-00	B010100	B019999	1	FRAME,IMPLOSION SHIELD
	426-0384-01	B020000		1	FRAME,IMPLOSION SHIELD
					(ATTACHING PARTS)
-8	210-0445-00			4	NUT,HEX.,10-32 X 0.375 INCH
-9	361-0168-00			4	SPACER,SLEEVE
-10	344-0233-00	B010100	B019999X	4	CLIP,GROUNDING,CRT
					- - - * - - -
-11	337-1482-00			1	SHIELD,IMPLOSION
-12	386-2100-00			-	SUPPORT,CRT,FRONT
					(ATTACHING PARTS)
	211-0507-00			4	SCREW,6-32 X 0.312 INCH,PHS (NOT SHOWN)
	210-0006-00			4	WASHER,LOCK,INTERNAL,0.146 ID X 0.283 INCH OD
					- - - * - - -
-13	- - - - - - -			1	CRT
	- - - - - - -			-	CRT INCLUDES:
-14	354-0316-01			1	RING,CRT MOUNTING
	136-0538-00			1	SOCKET ASSEMBLY,ANODE
	- - - - - - -			-	SOCKET ASSEMBLY INCLUDES:
-15	131-1188-00			1	CONNECTOR,PLUG,7 CONTACT
-16	131-1187-00			2	CONNECTOR COVER
-17	175-0830-00			FT	WIRE,ELECTRICAL,7 WIRE RIBBON,0.792 FT
-18	131-0271-00			1	SOCKET,TUBE,7 PIN
-19	337-1519-00			1	SHIELD,CRT,FRONT
					(ATTACHING PARTS)
-20	211-0507-00			4	SCREW,6-32 X 0.312 INCH,PHS
					- - - * - - -
-21	348-0013-00			8	FOOT,RUBBER,BLACK
-22	386-2097-00			1	SUPPORT,CRT,CENTER
					(ATTACHING PARTS)
	212-0023-00			2	SCREW,8-32 X 0.375 INCH,PHS
	210-0008-00			2	WASHER,LOCK,INTERNAL,0.172 ID X 0.331 INCH OD
					- - - * - - -
-23	- - - - - - -			1	CIRCUIT BOARD ASSY--HARD COPY A9
	- - - - - - -			-	CIRCUIT BOARD ASSEMBLY INCLUDES:
-24	214-0579-00			8	PIN,TEST POINT
-25	131-0589-00			7	TERMINAL,PIN,0.50 INCH LONG
	131-1233-00			7	TERMINAL,PIN,0.34 INCH LONG

FIGURE 2 FRONT & CRT (cont)

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Qty	Description 1 2 3 4 5
2-26	352-0125-00			1	HOLDER,TOROID,PLASTIC
-27	214-0506-00			1	PIN,CONNECTOR,0.375 INCH LONG
-28	136-0058-00			1	SOCKET,TUBE,7 PIN
					(ATTACHING PARTS)
-29	211-0116-00			2	SCREW,SEMS,4-40 X 0.312 INCH,PHB
					- - - * - - -
-30	348-0132-00			1	LINER,YOKE
-31	119-0422-00			1	YOKE ASSEMBLY,CRT
	- - - - - -			-	YOKE ASSEMBLY INCLUDES:
-32	348-0012-00			1	GROMMET,PLASTIC,0.625 INCH
-33	131-0621-00			4	CONNECTOR,TERMINAL
-34	352-0200-00			1	HOLDER,TERMINAL CONNECTOR,4 WIRE
-35	343-0413-00			2	CLAMP HALF,CRT YOKE
					(ATTACHING PARTS FOR EACH)
-36	212-0023-00			1	SCREW,8-32 X 0.375 INCH,PHS
-37	211-0511-00			1	SCREW,6-32 X 0.50 INCH,PHS
					- - - * - - -
-38	337-1520-00	B010100	B039999	1	SHIELD,CRT,REAR
	337-1520-02	B040000		1	SHIELD,CRT,REAR
					(ATTACHING PARTS)
-39	210-0458-00			2	NUT,KEPS,8-32 X 0.344 INCH
-40	210-0805-00			2	WASHER,FLAT,0.204 ID X 0.438 INCH OD
	407-1418-00	XB040000		1	BRACKET,YOKE MOUNTING
					- - - * - - -
-41	- - - - - -			1	CIRUCIT BOARD ASSY--DEFLECTION AMP & STORAGE A4
	- - - - - -			-	CIRCUIT BOARD ASSEMBLY INCLUDES:
-42	131-0589-00			114	TERMINAL,PIN,0.46 INCH LONG
	131-0608-00			3	TERMINAL,PIN,0.365 INCH LONG
-43	131-0993-00			1	LINK,TERMINAL CONNECTING
	- - - - - -			-	LINK INCLUDES:
	131-0707-00			2	CONNECTOR,TERMINAL
	352-0169-00			1	HOLDER,TERMINAL CONNECTOR,2 WIRE
-44	- - - - - -			1	TRANSISTOR
					(ATTACHING PARTS)
-45	210-0586-00			2	NUT,KEPS,4-40 X 0.25 INCH
-46	355-0159-00			2	TERMINAL,STUD,HEX.
					- - - * - - -
-47	214-1795-00			1	HEATSINK
					(ATTACHING PARTS)
-48	211-0601-00			6	SCREW,SEMS,6-32 X 0.312 INCH,PHB
-49	384-0519-00			6	ROD,HEX.,0.562 INCH LONG
-50	211-0507-00			6	SCREW,6-32 X 0.312 INCH,PHS
					- - - * - - -
-51	- - - - - -			4	TRANSISTOR
					(ATTACHING PARTS FOR EACH)
-52	211-0511-00			1	SCREW,6-32 X 0.50 INCH,PHS
-53	210-0803-00			1	WASHER,FLAT,0.15 ID X 0.312 INCH OD
-54	210-0811-00			1	WASHER,FIBER,SHOULDERED,#6
-55	386-0143-00			1	PLATE,INSULATOR,0.80 X 0.135 INCHES
-56	210-0071-00			1	WASHER,SPRING TENSION
-57	210-0407-00			1	NUT,HEX.,6-32 X 0.25 INCH
					- - - * - - -

FIGURE 2 FRONT & CRT (cont)

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Qty	1 2 3 4 5 Description
2-58	------			4	TRANSISTOR
					(ATTACHING PARTS FOR EACH)
-59	211-0511-00			2	SCREW,6-32 X 0.50 INCH,PHS
-60	342-0136-00			1	INSULATOR,WASHER,TRANSISTOR
-61	210-0967-00			2	WASHER,PLASTIC,0.157 ID X 0.375 INCH OD
-62	210-0803-00			2	WASHER,FLAT,0.15 ID X 0.375 INCH OD
-63	210-0202-00			1	TERMINAL,LUG,SOLDER,SE #6
-64	210-0407-00			1	NUT,HEX.,6-32 X 0.25 INCH
-65	210-0457-00			1	NUT,KEPS,6-32 X 0.312 INCH
					--- * ---
-66	131-0707-00			8	CONNECTOR,TERMINAL
-67	352-0161-00			4	HOLDER,TERMINAL CONNECTOR,3 WIRE
-68	175-0826-00			FT	WIRE,ELECTRICAL,3 WIRE RIBBON,3.833 FT
					(ATTACHING PARTS)
-69	211-0507-00			2	SCREW,6-32 X 0.312 INCH, PHS
-70	210-0006-00			2	WASHER,LOCK,INTERNAL,0.146 ID X 0.286 INCH OD
-71	385-0122-00			2	ROD,METALLIC,HEX.,0.938 INCH LONG
					--- * ---
-72	386-2413-00			1	SUPPORT,CRT,MAIN
					(ATTACHING PARTS)
-73	212-0023-00			2	SCREW,8-32 X 0.375 INCH,PHS
-74	210-0008-00			2	WASHER,LOCK,INTERNAL,0.172 ID X 0.331 INCH OD
	211-0541-00			3	SCREW,6-32 X 0.25 INCH,100 DEG. CSK,FHS
					--- * ---
-75	260-1274-00			1	SWITCH,ROCKER,MOMENTARY
					(ATTACHING PARTS)
-76	210-0406-00			2	NUT,HEX.,4-40 X 0.188 INCH
-77	210-0004-00			2	WASHER,LOCK,INTERNAL,0.12 ID X 0.26 INCH OD
-78	166-0024-00			2	TUBE,SPACER,0.125 INCH LONG
					--- * ---
-79	260-1334-00			1	SWITCH,ROCKER
					(ATTACHING PARTS)
-80	210-0406-00			2	NUT,HEX.,4-40 X 0.188 INCH
-81	210-0004-00			2	WASHER,LOCK,INTERNAL,0.12 ID X 0.26 INCH OD
-82	166-0024-00			2	TUBE,SPACER,0.125 INCH LONG
					--- * ---

FIGURE 3 PEDESTAL

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Qty	1 2 3 4 5 Description
3-1	437-0130-00			1	CABINET,PEDASTAL UNIT
	- - - - - - -			-	CABINET INCLUDES:
-2	220-0625-00			18	NUT,CLIP-ON
-3	200-1518-00			1	COVER,FRONT,ACCESS,HINGED
	- - - - - - -			-	COVER INCLUDES:
-4	348-0102-00			2	PAD,CUSHIONING,10 INCHES LONG
-5	214-0329-00			2	THUMBSCREW,6-32 X 0.656 INCH,W/STANDOFF
					(ATTACHING PARTS)
-6	213-0302-00			4	SCREW,6-32 X 0.50 INCH,PHS
					- - - * - - -
-7	352-0102-00			1	HOLDER,FUSE
					(ATTACHING PARTS)
-8	210-0406-00			2	NUT,HEX.,4-40 X 0.187 INCH
-9	210-0004-00			2	WASHER,LOCK,INTERNAL,0.12 ID X 0.26 INCH OD
					- - - * - - -
-10	386-2417-00			1	PLATE,MOUNTING
					(ATTACHING PARTS)
-11	212-0043-00			4	SCREW,8-32 X 0.50 INCH, 100 DEG. CSK,FHS
					- - - * - - -
-12	200-1288-00			1	COVER,REAR
					(ATTACHING PARTS)
-13	213-0302-00			4	SCREW,6-32 X 0.50 INCH,PHS
					- - - * - - -
-14	200-1350-00			1	COVER,PLATE
					(ATTACHING PARTS)
-15	211-0638-00			4	SCREW,6-32 X 0.738 INCH,THS
					- - - * - - -
-16	124-0264-00			1	STRIP,TRIM
					(ATTACHING PARTS)
-17	210-0457-00			2	NUT,KEPS,6-32 X 0.312 INCH
					- - - * - - -
-18	432-0073-00			1	BASE,PEDESTAL UNIT
					(ATTACHING PARTS)
-19	213-0163-00			4	SCREW,0.25-32 X 0.625 INCH,HSS
-20	210-0853-00			4	WASHER,FLAT,0.266 ID X 0.50 INCH OD
					- - - * - - -
-21	348-0292-00			4	FOOT,BASE
					(ATTACHING PARTS FOR EACH)
-22	210-0411-00			1	NUT,HEX.,0.25-0.20 X 0.438 INCH
					- - - * - - -
-23	200-1378-00			4	CAP,BLACK PLASTIC
-24	343-0005-00			2	CLAMP,CABLE,PLASTIC,0.438 INCH
-25	343-0003-00			2	CLAMP,CABLE,PLASTIC,0.25 INCH
					(ATTACHING PARTS FOR EACH)
-26	210-0457-00			1	NUT,KEPS,6-32 X 0.312 INCH
-27	210-0863-00			1	WASHER,D-SHAPE,0.191 ID X 0.515 INCH OD
					- - - * - - -

FIGURE 3 PEDESTAL (cont)

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Qty	Description 1 2 3 4 5
3-28	351-0238-00			2	GUIDE,CIRCUIT CARD
					(ATTACHING PARTS FOR EACH)
-29	211-0507-00			6	SCREW,6-32 X 0.312 INCH,PHS
-30	210-0457-00			6	NUT,KEPS,6-32 X 0.312 INCH
					- - - * - - -
-31	255-0334-00			IN	PLASTIC CHANNEL,4.875 INCHES LONG
-32	343-0015-00			1	CLAMP,CABLE,STAINLESS STEEL,0.50 INCH
					(ATTACHING PARTS)
-33	210-0457-00			1	NUT,KEPS,6-32 X 0.312 INCH
					- - - * - - -
-34	348-0056-00			1	GROMMET,PLASTIC,0.375 INCH
-35	260-1179-01			1	SWITCH,POWER
					(ATTACHING PARTS)
-36	211-0541-00			2	SCREW,6-32 X 0.25 INCH, 100 DEG. CSK,FHS
					- - - * - - -
-37	334-1917-00			1	LABEL,INFORMATION
-38	179-1758-00			1	WIRING HARNESS,AC #1
	- - - - - -			-	WIRING HARNESS INCLUDES:
-39	131-0946-00			1	CONNECTOR SHELL,FEMALE
-40	131-0945-00			4	CONTACT,ELECTRICAL,MALE
	179-1949-01			1	WIRING HARNESS,MAIN
	- - - - - -			-	WIRING HARNESS INCLUDES:
-41	131-0621-00			112	CONNECTOR,TERMINAL
	131-0622-00			11	CONNECTOR,TERMINAL
	131-0792-00			17	CONNECTOR,TERMINAL
-42	352-0197-00			3	HOLDER,TERMINAL CONNECTOR,1 WIRE
-43	352-0198-00			5	HOLDER,TERMINAL CONNECTOR,2 WIRE
-44	352-0199-00			6	HOLDER,TERMINAL CONNECTOR,3 WIRE
-45	352-0200-00			2	HOLDER,TERMINAL CONNECTOR,4 WIRE
-46	352-0201-00			1	HOLDER,TERMINAL CONNECTOR,5 WIRE
-47	352-0202-00			4	HOLDER,TERMINAL CONNECTOR,6 WIRE
-48	352-0203-00			5	HOLDER,TERMINAL CONNECTOR,7 WIRE
-49	352-0205-00			4	HOLDER,TERMINAL CONNECTOR,9 WIRE
-50	352-0206-00			2	HOLDER,TERMINAL CONNECTOR,10 WIRE
-51	200-0811-00			1	COVER,SOCKET TERMINALS
-52	136-0271-00			1	SOCKET,ELECTRON TUBE

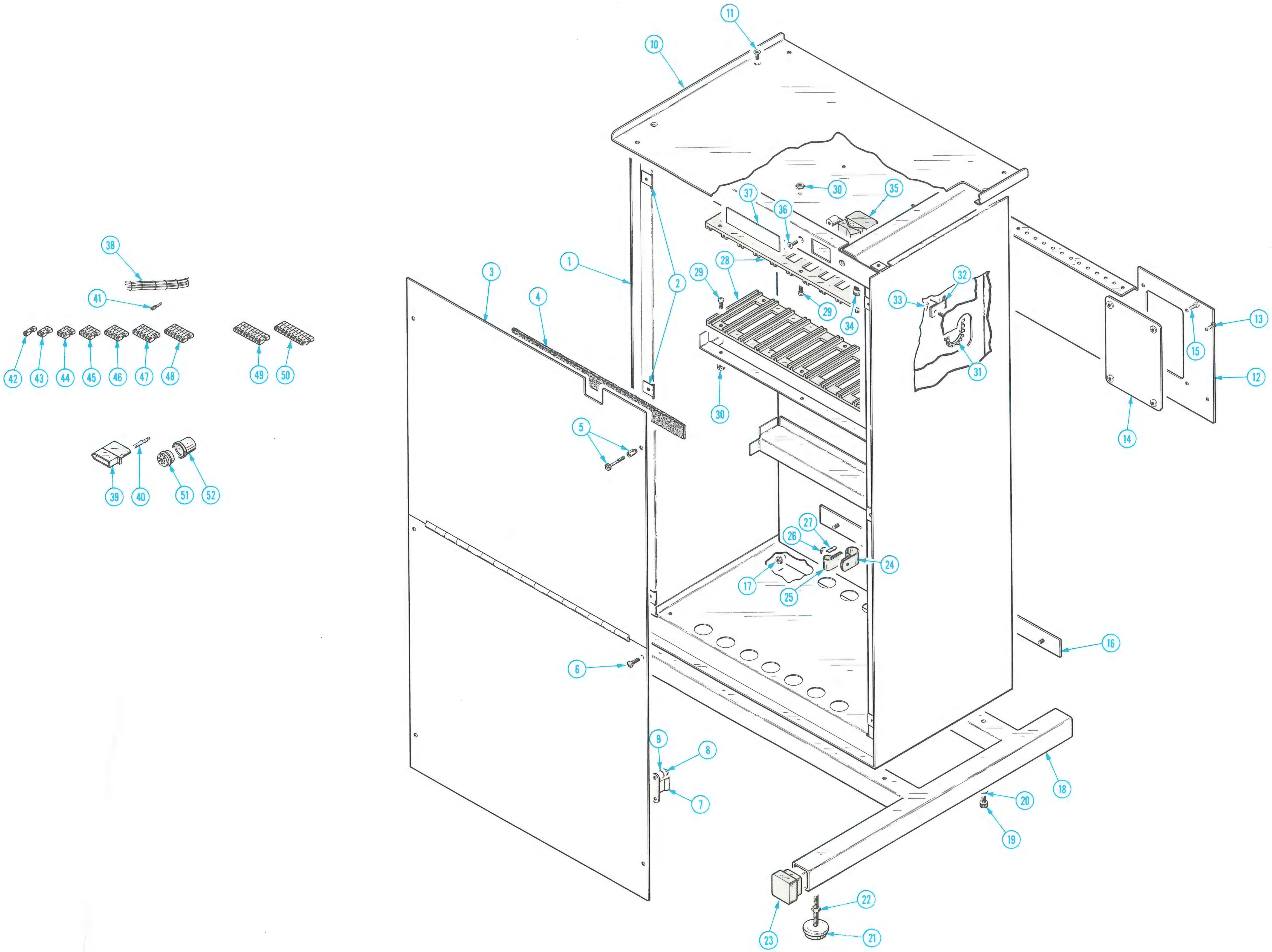


FIG. 3 PEDESTAL

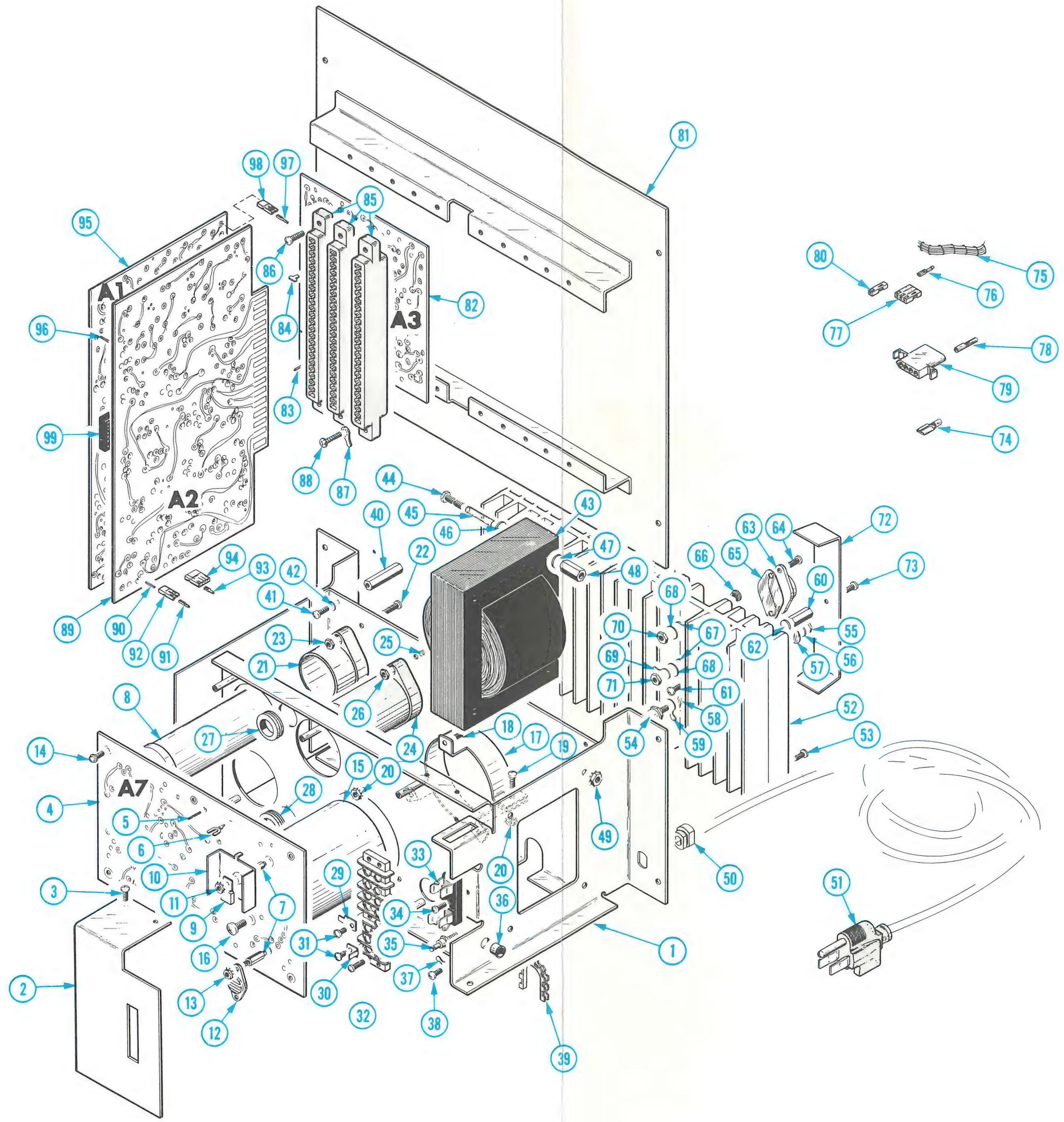


FIG. 4 POWER SUPPLY

FIGURE 4 POWER SUPPLY

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Qty	Description 1 2 3 4 5
4-	620-0225-00			1	LOW VOLTAGE POWER SUPPLY
	- - - - - -			-	POWER SUPPLY INCLUDES:
-1	437-0129-00			1	CHASSIS,POWER SUPPLY
-2	337-1629-00			1	SHIELD,FUSE
					(ATTACHING PARTS)
-3	211-0097-00			2	SCREW,4-40 X 0.312 INCH,PHS
					- - - * - - -
-4	- - - - - -			1	CIRCUIT BOARD ASSY--LOW VOLTAGE POWER A7
	- - - - - -			-	CIRCUIT BOARD ASSEMBLY INCLUDES:
-5	131-0589-00			40	TERMINAL,PIN,0.46 INCH LONG
-6	344-0154-00			6	CLIP,FUSE
-7	355-0159-00			3	TERMINAL,STUD
-8	- - - - - -			3	CAPACITOR
-9	- - - - - -			1	TRANSISTOR
-10	214-1671-00			1	HEATSINK
					(ATTACHING PARTS)
-11	210-0586-00			1	NUT,KEPS,4-40 X 0.25 INCH
	210-0004-00			1	WASHER,LOCK,INTERNAL,0.12 ID X 0.26 INCH OD
					- - - * - - -
-12	- - - - - -			1	TRANSISTOR
					(ATTACHING PARTS)
-13	210-0586-00			2	NUT,KEPS,4-40 X 0.25 INCH
					(ATTACHING PARTS)
-14	211-0116-00			6	SCREW,SEMS,4-40 X 0.312 INCH,PHB
					- - - * - - -
-15	- - - - - -			1	CAPACITOR
					(ATTACHING PARTS)
-16	212-0518-00			2	SCREW,10-32 X 0.312 INCH,PHS
					- - - * - - -
-17	343-0064-00			1	CLAMP,CAPACITOR
					(ATTACHING PARTS)
-18	211-0510-00			3	SCREW,6-32 X 0.375 INCH,PHS
-19	211-0513-00			1	SCREW,6-32 X 0.625 INCH,PHS
-20	210-0457-00			4	NUT,KEPS,6-32 X 0.312 INCH
					- - - * - - -
-21	432-0048-00			2	BASE,CAPACITOR MOUNTING,1.375 INCHES HIGH
					(ATTACHING PARTS FOR EACH)
-22	211-0513-00			2	SCREW,6-32 X 0.625 INCH,PHS
-23	210-0407-00			2	NUT,HEX.,6-32 X 0.25 INCH
					- - - * - - -
-24	432-0048-01			1	BASE,CAPACITOR MOUNTING,2.375 INCHES HIGH
					(ATTACHING PARTS)
-25	211-0513-00			2	SCREW,6-32 X 0.625 INCH,PHS
-26	210-0407-00			2	NUT,HEX.,6-32 X 0.25 INCH
					- - - * - - -

FIGURE 4 POWER SUPPLY (cont)

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Qty	1 2 3 4 5 Description
4-27	348-0012-00			1	GROMMET,RUBBER,0.625 INCH DIAMETER
-28	348-0006-00			2	GROMMET,RUBBER,0.75 INCH DIAMETER
-29	210-0292-00			10	TERMINAL,LUG,SOLDER
-30	131-1247-00			9	TERMINAL,LUG,SOLDERLESS
-31	124-0006-00			1	STRIP,TERMINAL,W/HARDWARE
					(ATTACHING PARTS)
-32	211-0012-00			2	SCREW,4-40 X 0.375 INCH,PHS
					- - - * - - -
-33	352-0031-00			1	HOLDER,FUSE
					(ATTACHING PARTS)
-34	211-0510-00			1	SCREW,6-32 X 0.375 INCH,PHS
					- - - * - - -
-35	129-0006-00			1	POST,CONNECTOR
-36	348-0056-00			1	GROMMET,PLASTIC,0.375 INCH DIAMETER
-37	210-0201-00			1	TERMINAL,LUG,SOLDER
					(ATTACHING PARTS)
-38	213-0044-00			1	SCREW,THREAD FORMING,5-32 X 0.188 INCH,PHS
					- - - * - - -
-39	255-0334-00			IN	PLASTIC CHANNEL,4.50 INCHES
-40	385-0122-00			6	ROD,HEX.,0.938 INCH LONG
					(ATTACHING PARTS FOR EACH)
-41	211-0510-00			1	SCREW,6-32 X 0.375 INCH,PHS
-42	210-0006-00			1	WASHER,LOCK,INTERNAL,0.146 ID X 0.286 INCH OD
					- - - * - - -
-43	- - - - - -			1	TRANSFORMER
	- - - - - -			-	TRANSFORMER INCLUDES:
-44	212-0515-00			4	SCREW,10-32 X 2.25 INCHES,HHS
-45	166-0226-00			4	TUBE,INSULATING,1.125 INCHES LONG
-46	210-0812-00			4	WASHER,FIBER,#10
-47	210-0805-00			4	WASHER,FLAT,0.204 ID X 0.438 INCH OD
-48	384-0597-00			4	ROD,SPACER
					(ATTACHING PARTS)
-49	220-0410-00			4	NUT,KEPS,10-32 X 0.375 INCH
					- - - * - - -
-50	358-0161-00			1	BUSHING,HEYCO
-51	161-0033-07			1	CABLE ASSEMBLY,POWER
-52	214-1666-00			1	HEATSINK
					(ATTACHING PARTS)
-53	211-0537-00			6	SCREW,6-32 X 0.375 INCH,THS
					- - - * - - -
-54	- - - - - -			2	DIODE
					(ATTACHING PARTS FOR EACH)
-55	220-0410-00			1	NUT,KEPS,10-32 X 0.375 INCH
-56	210-0805-00			1	WASHER,FLAT,0.204 ID X 0.438 INCH OD
-57	210-0909-00			2	WASHER,MICA
-58	210-0910-00			1	WASHER INSULATOR,PLASTIC,0.188 ID X 0.312" OD
-59	210-0224-00			1	TERMINAL,LUG,SOLDER,#10
					- - - * - - -

FIGURE 4 POWER SUPPLY (cont)

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Qty	1 2 3 4 5 Description
4-60	384-0519-00			2	ROD,SPACER
					(ATTACHING PARTS FOR EACH)
-61	211-0510-00			1	SCREW,6-32 X 0.375 INCH,PHS
-62	210-0006-00			1	WASHER,LOCK,INTERNAL,0.146 ID X 0.283 INCH OD
					- - - * - - -
-63	- - - - - -			3	TRANSISTOR
					(ATTACHING PARTS FOR EACH)
-64	211-0513-00			2	SCREW,6-32 X 0.625 INCH,PHS
-65	386-0978-00			1	INSULATOR,PLATE
-66	210-0910-00			2	WASHER INSULATOR,PLASTIC,0.188 ID X 0.312
	- - - - - -			-	INCH OD
-67	210-0967-00			2	WASHER,PLASTIC,SHOULDERED,0.157 ID X 0.375
	- - - - - -			-	INCH OD
-68	210-0803-00			2	WASHER,FLAT,0.15 ID X 0.375 INCH OD
-69	210-0202-00			1	TERMINAL,LUG,SOLDER,SE #6
-70	210-0457-00			1	NUT,KEPS,6-32 X 0.312 INCH
-71	210-0407-00			1	NUT,HEX.,6-32 X 0.25 INCH
					- - - * - - -
-72	200-1330-00			2	COVER,TRANSISTOR
					(ATTACHING PARTS FOR EACH)
-73	211-0537-00			1	SCREW,6-32 X 0.375 INCH,THS
					- - -* - - -
-74	131-0861-00			4	TERMINAL,QUICK DISCONNECT
-75	179-1760-00			1	WIRING HARNESS,POWER #1
	- - - - - -			-	WIRING HARNESS INCLUDES:
-76	131-0621-00			3	CONNECTOR,TERMINAL
-77	352-0199-00			1	HOLDER,TERMINAL CONNECTOR,3 WIRE
	179-1759-00			1	WIRING HARNESS,A.C. #2
	- - - - - -			-	WIRING HARNESS INCLUDES:
-78	131-0948-00			4	CONTACT,ELECTRICAL,FEMALE
-79	131-0947-00			1	CONNECTOR SHELL,MALE
	179-1761-00			1	WIRING HARNESS,POWER #2
	- - - - - -			-	WIRING HARNESS INCLUDES:
	131-0621-00			4	CONNECTOR,TERMINAL
-80	352-0197-00			1	HOLDER,TERMINAL CONNECTOR,1 WIRE
	352-0199-00			1	HOLDER,TERMINAL CONNECTOR,3 WIRE
					(ATTACHING PARTS)
	213-0302-00			4	SCREW,6-32 X 0.50 INCH,PHS
	211-0507-00			2	SCREW,6-32 X 0.312 INCH,PHS
	210-0006-00			2	WASHER,LOCK,INTERNAL,0.146 ID X 0.286 INCH OD
					- - - * - - -
-81	441-1037-00			1	CHASSIS,CIRCUIT CARD
					(ATTACHING PARTS)
	213-0302-00			4	SCREW,6-32 X 0.375 INCH,THS
					- - - * - - -

FIGURE 4 POWER SUPPLY (cont)

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Qty	Description 1 2 3 4 5
4-82	- - - - - -			1	CIRCUIT BOARD ASSY--MOTHER A3
	- - - - - -			-	CIRCUIT BOARD ASSEMBLY INCLUDES:
-83	131-0589-00			41	TERMINAL,PIN
-84	131-1148-00			6	KEY,CONNECTOR
-85	131-1147-00			3	CONNECTOR,72 PIN
					(ATTACHING PARTS)
-86	211-0511-00			6	SCREW,6-32 X 0.50 INCH,PHS
					- - - * - - -
-87	210-0202-00			1	TERMINAL,LUG,SOLDER,SE #6
					(ATTACHING PARTS)
-88	211-0507-00			1	SCREW,6-32 X 0.312 INCH,PHS
					- - - * - - -
-89	- - - - - -			1	CIRCUIT CARD ASSY--TC-2 TERMINAL CONTROL A2
	- - - - - -			-	CIRCUIT CARD ASSEMBLY INCLUDES:
-90	131-0608-00			15	TERMINAL,PIN,0.365 INCH LONG
	131-0787-00			13	TERMINAL,PIN,0.64 INCH LONG
	131-0993-00			1	LINK,TERMINAL CONNECTOR
	- - - - - -			-	LINK INCLUDES:
-91	131-0707-00			2	CONNECTOR,TERMINAL
-92	352-0169-00			1	HOLDER,TERMINAL CONNECTOR,2 WIRE
	131-1207-00			1	LINK,TERMINAL CONNECTOR
	- - - - - -			-	LINK INCLUDES:
-93	131-0707-00			4	CONNECTOR,TERMINAL
-94	352-0162-00			1	HOLDER,TERMINAL CONNECTOR,4 WIRE
-95	- - - - - -			1	CIRCUIT CARD ASSY--TC-1 TERMINAL CONTROL A1
	- - - - - -			-	CIRCUIT CARD ASSEMBLY INCLUDES:
-96	131-0608-00			6	TERMINAL,PIN
	131-0608-00[1]			3	TERMINAL,PIN
	131-0993-00			3	LINK,TERMINAL CONNECTOR
	131-0993-00[1]			1	LINK,TERMINAL CONNECTOR
	- - - - - -			-	EACH LINK INCLUDES:
-97	131-0707-00			8	CONNECTOR,TERMINAL
-98	352-0161-00			1	HOLDER,TERMINAL CONNECTOR,3 WIRE
-99	136-0432-00			3	SOCKET,INTEGRATED CIRCUIT,24 PIN

[1]Used with 02 suffix board only.

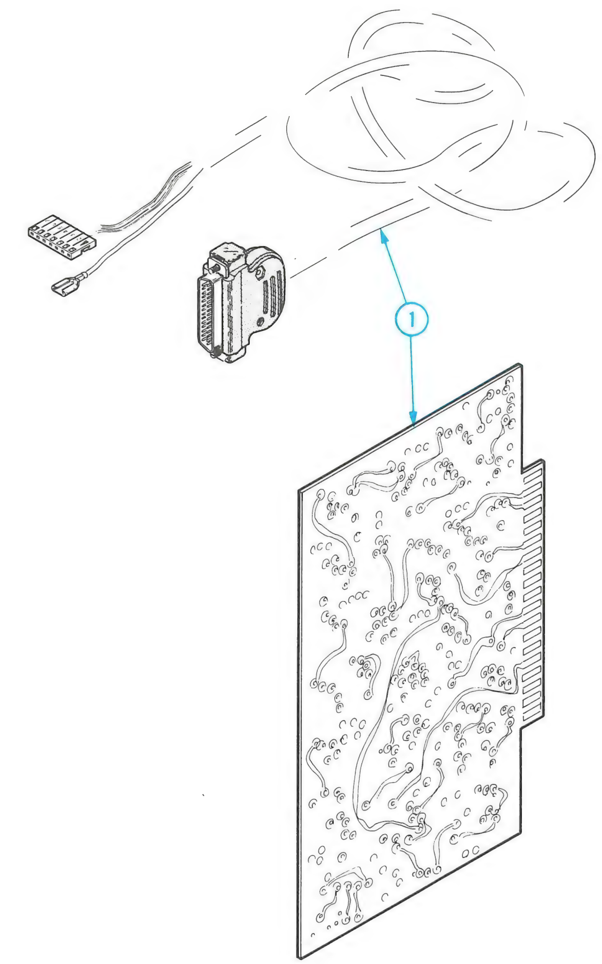
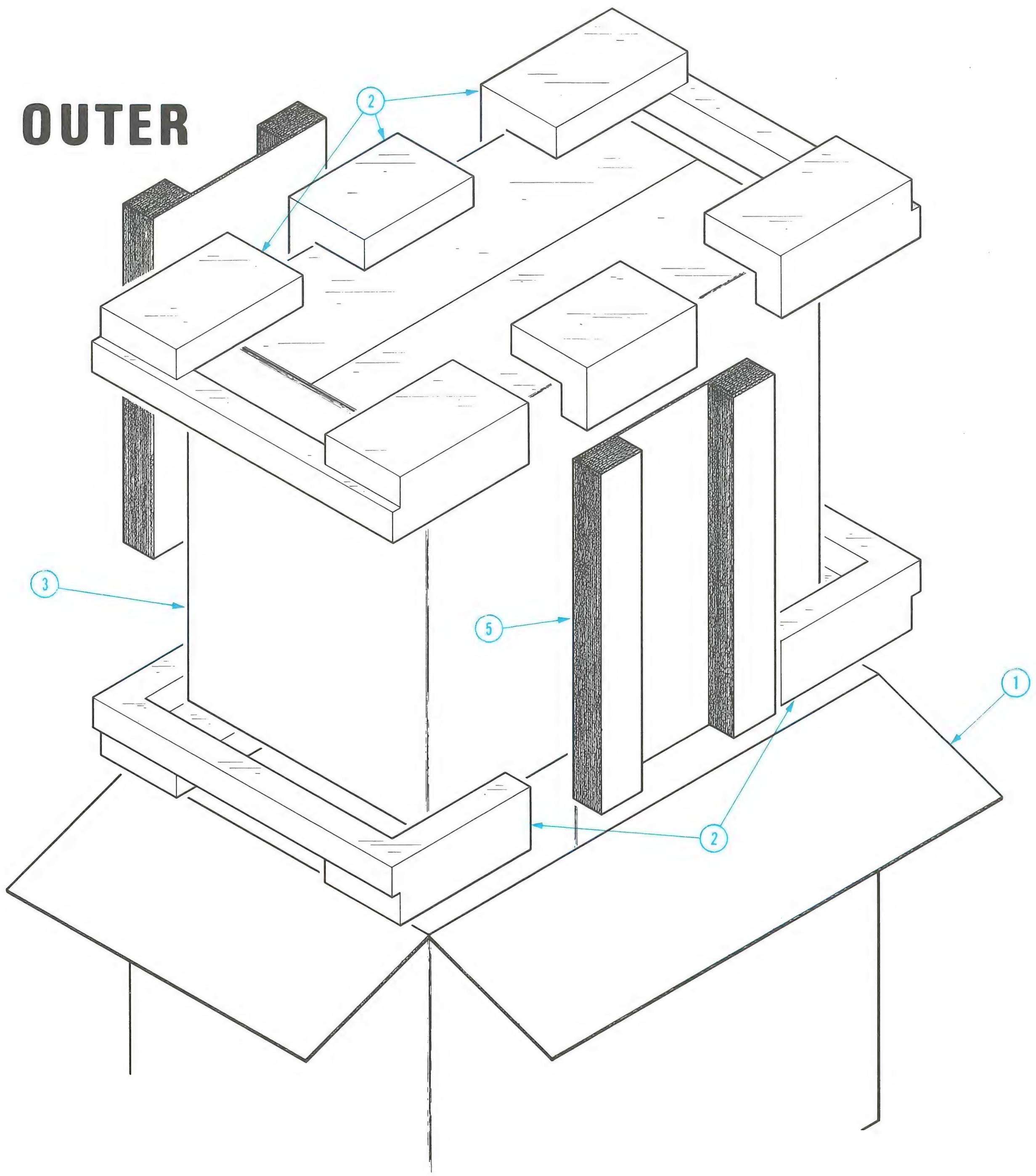


Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Qty	1 2 3 4 5 Description
5-1	021-0065-00			1	DATA COMMUNICATIONS INTERFACE
	070-1458-00			1	MANUAL, instruction, data communications interface
	070-1460-00			1	MANUAL, users, 4012



REPACKAGING

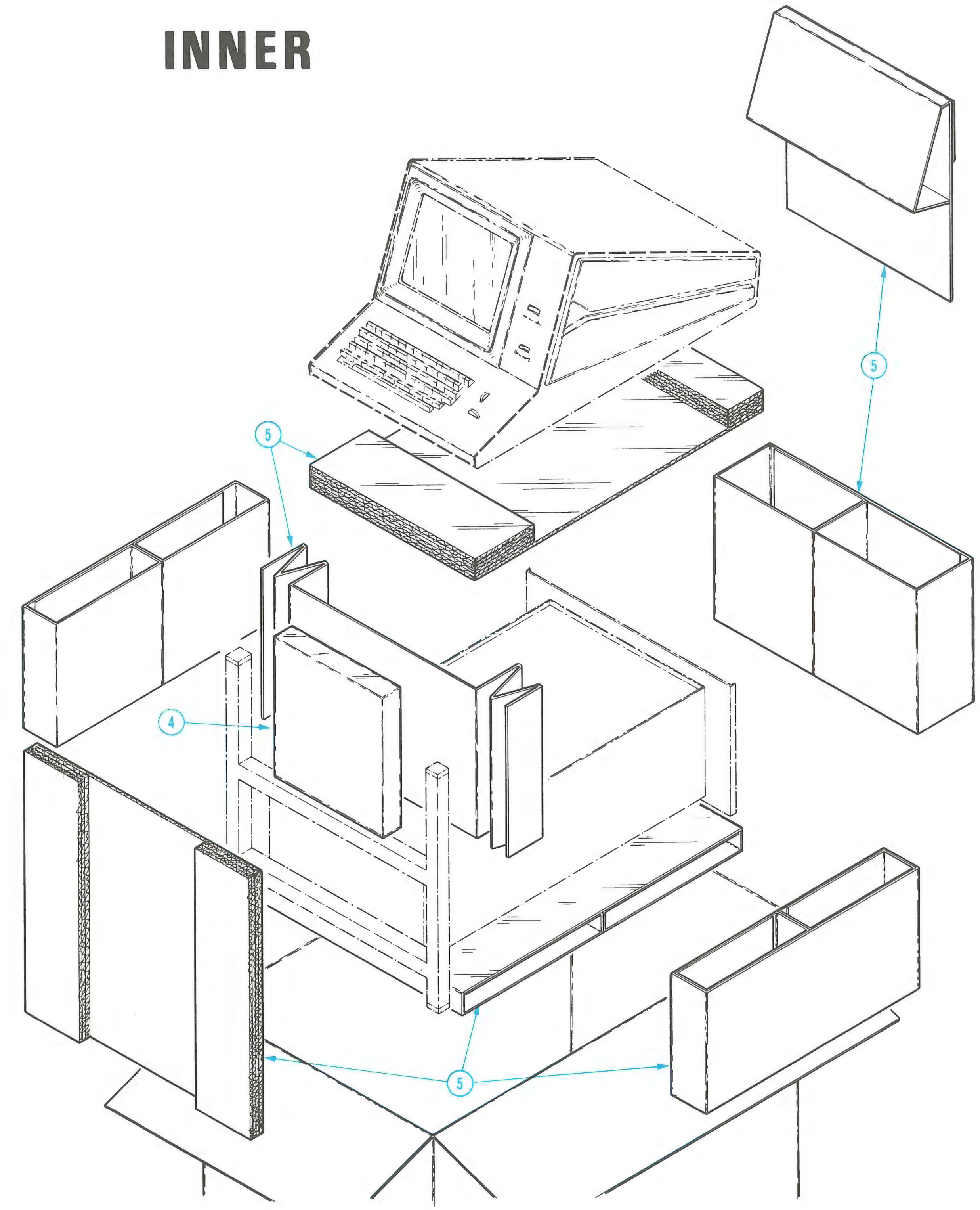


FIG. 6 REPACKAGING

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Qty	1 2 3 4 5 Description
6-1	065-0189-00			1	CARTON ASSEMBLY
	- - - - - - - - - -			-	carton assembly includes:
-1	004-0854-00			1	CARTON, outer
-2	004-0276-00			2 1/2	FRAME
-3	004-0855-00			1	CARTON, inner
-4	004-0418-00			1	CARTON, 9.5 x 12 x 2 inches
-5	004-1159-00			1	PAD-SET

MANUAL CHANGE INFORMATION

At Tektronix, we continually strive to keep up with latest electronic developments by adding circuit and component improvements to our instruments as soon as they are developed and tested.

Sometimes, due to printing and shipping requirements, we can't get these changes immediately into printed manuals. Hence, your manual may contain new change information on following pages.

A single change may affect several sections. Sections of the manual are often printed at different times, so some of the information on the change pages may already be in your manual. Since the change information sheets are carried in the manual until ALL changes are permanently entered, some duplication may occur. If no such change pages appear in this section, your manual is correct as printed.

4012

4013

TEXT CORRECTION

Page, 6-5 TABLE 6-2

CHANGE last line to read:

J20	4	K BIT 5 (b5)	80	10	A8	9-18

Page 6-6 TABLE 6-2

CHANGE 6th line item to read:

J21	3	K BIT 6 (b6)	80	11	A8	9-17

Page 6-10 TABLE 6-7

CHANGE 5th line item to read:

J80	5	+5V	21	4	A7	2-0,2-0,9-16

CHANGE 8th line item to read:

J80	8	GND	20	1		0-9,9-0 shield, O-N

CHANGE 10th line item to read:

J80	10	K BIT 5 (b5)	20	4	A8	9-18

CHANGE 11th line item to read:

J80	11	K BIT 6 (b6)	21	3	A8	9-17

4012 Service

4013 Service

ELECTRICAL PARTS LIST CHANGE

CHANGE TO:

A4	670-2571-04	CIRCUIT BOARD ASSEMBLY, DEFLECTION AMPL & STORAGE
R647	315-0102-00	1K OHM, 0.25W, 5%
U555B	156-0149-01	DUAL 4-INPUT, NAND SN7413N

ADD:

R555	315-0102-00	1K OHM,0.25W, 5%
R648	315-0102-00	1K OHM, 0.25W, 5%

REMOVE:

C169	283-0000-00	0.001 μF, CER, 500 V, +80-20%
C270	283-0110-00	0.005 μF, CER, 150 V
C472	290-0536-00	10 μF, CER, 500 V, +80-20%
C549	283-0010-00	0.05 μF, CER, 50 V
C654	283-0000-00	0.001 μF, CER, 500 V, +80-20%
R169	315-0101-00	100 OHM, 0.25W, 5%
R269	315-0201-00	200 OHM, 0.25W, 5%
R369	315-0472-00	4.7K OHM, 0.25W, 5%
R549	315-0822-00	8.2K OHM, 0.25W, 5%
R654	315-0101-00	100 OHM, 0.25W, 5%

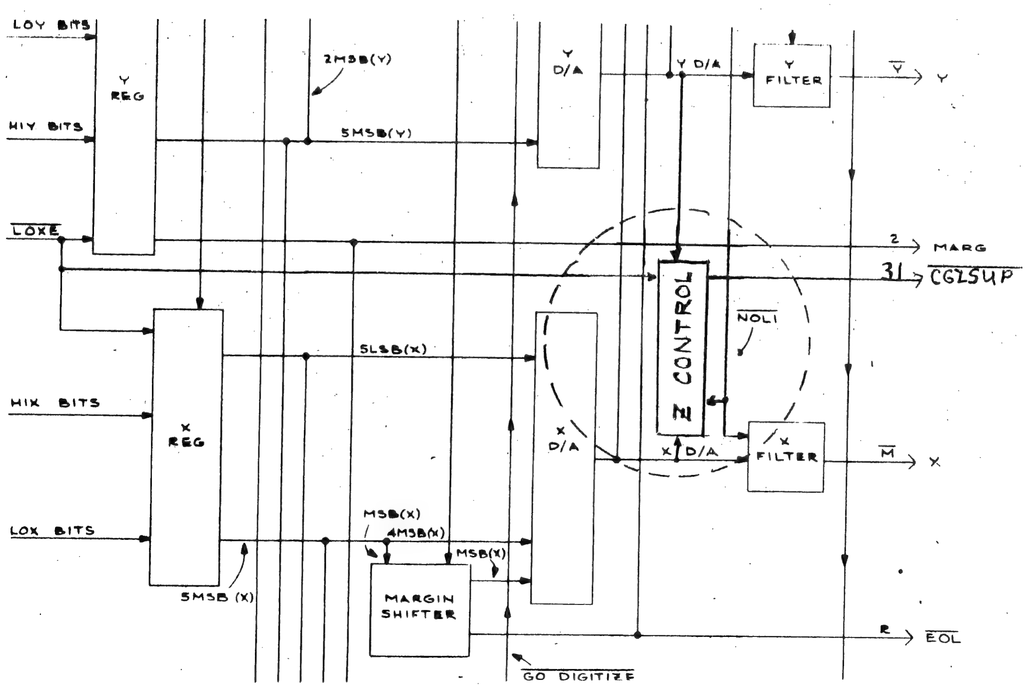
Page 6-21

Left Column, immediately before the topic titled "Returning to Alpha Mode" insert the following:

A Z Control circuit is contained on TC-2 circuit cards #670-1729-04 and above. This chops the Z signal during short vector drawing to reduce the vector intensity, making short vector intensity more consistent with long vector intensity. The $\overline{\text{LOXE}}$, $\overline{\text{NOLI}}$, X D/A, Y D/A, and three clock signals (not shown) are fed into the circuit to hold $\overline{\text{CGZ SUP}}$ high for vectors more than approximately one-half inch long, and to place a 12 1/2% duty cycle high on the $\overline{\text{CGZSUP}}$ line while vectors less than approximately one-half inch are being drawn.

Fig. 6-9

Right-middle. Change as indicated in the attached Partial Fig. 6-9.



Partial Fig. 6-9 GRAPHIC MODES BLOCK DIAGRAM

Page 6-34

Right Column, immediately before the topic titled "Block Description", insert the following:

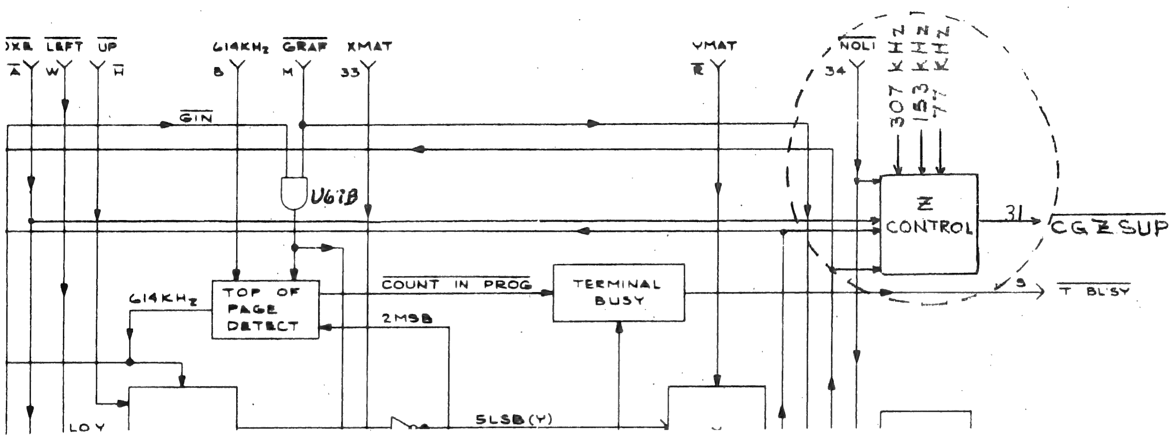
Z Control Circuit - (Circuit Cards 670-1729-04 and above) - Controls vector intensity when vectors less than approximately one-half inch long are being drawn.

Page 6-36

Right Column, immediately before the topic titled "Crosshair Generator", insert the following:

Z Control. This circuit is used only in Graph Mode while drawing vectors. It is then enabled by a high $\overline{\text{NOLI}}$ signal. When $\overline{\text{LOXE}}$ initiates a vector, the circuit becomes armed and a 10 μs delay is initiated. If the vector being drawn is less than approximately one-half inch, the three clock pulses (307 kHz, 153 kHz, and 77 kHz) combine to hold $\overline{\text{CGZSUP}}$ low for 11.4 μs out of every 13 μs. The 1.6 μs pulses generated while $\overline{\text{CGZSUP}}$ is high cause dots to be written on the screen. These dots are close enough together to appear as a continuous line. If the vector being drawn is more than approximately one-half inch long, the X D/A or Y D/A signal is large enough to reset the circuit before the 10 μs delay elapses, preventing $\overline{\text{CGZSUP}}$ from going low. The beam is then permitted to be left on during vector drawing.

Fig. 6-18 Top-right corner. Change part of Fig. 6-18 as shown in the attached Partial Fig. 6-18.



Partial Fig. 6-18. TC-2 DETAILED BLOCK DIAGRAM

Fig. 6-20 Add a line and the notation "TO Z CONTROL BOARD, FIG. 6-20A (TC-2 CARDS 670-1729-04 ONLY)" to each of the following points on the TC-2 schematic:

U39 pin 6 Right edge, 1/4 of way from top

U79 pin 6

$\overline{\text{LOXE}}$ input at pin A - Left edge, 1/4 of way from top

$\overline{\text{NOLI}}$ input at pin 34 - Left edge, 3/5 of way from top

U27A pin 15 near left edge, 3/4 of way from top

U29A pin 12

U34 pin 12

-15 V input at pin 14 - Left edge, 5/6 of way from top

+5 V input at pin S - Left edge, at bottom

GND input at pins A, 36

ADD: "CARDS #670-1729-04 AND BELOW" near the figure number in the bottom-right corner.

ADD: A new Fig. 6-20A as attached.

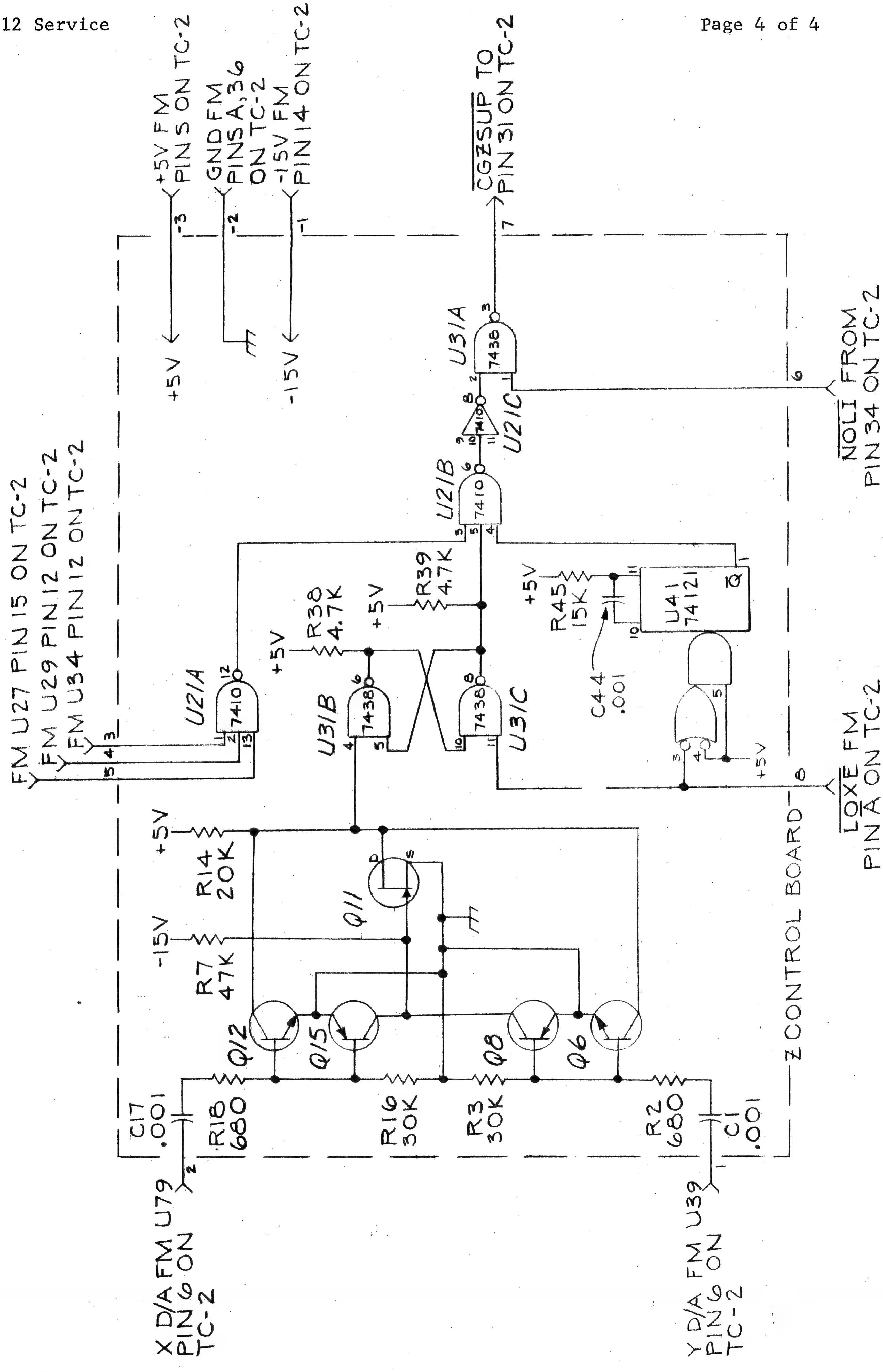


FIG. 6-20A. Z CONTROL BOARD
(PART OF TC-2 #670-1729-04)

ELECTRICAL PARTS LIST AND SCHEMATIC CORRECTIONS

A1 ASSEMBLY TC-1 (4010/R, 4010-1/R Only)

CHANGE TO:

A1	670-1728-03	TC-1 Circuit Card Assembly

ADD:

CR9	152-0075-00	Silicon	1N3258

REMOVE: (complete Bill of Materials)

A2	670-1729-02	CIRCUIT CARD ASSEMBLY, TC-2
A2	670-1729-04	CIRCUIT CARD ASSEMBLY, TC-2
	670-3084-00	CIRCUIT BOARD ASSEMBLY, Z CONTROL

ADD: (complete Bill of Materials as follows)

A2 ASSEMBLY TC-2

ASSEMBLY

A2	670-1729-05	CIRCUIT CARD ASSEMBLY, TC-2

CAPACITORS

C9	283-0068-00	0.01 μF, Cer, 500 V
C38	281-0546-00	330 pF, Cer, 500 V
C84	290-0512-00	22 μF, Elect, 15 V, 20%
C88	285-0596-00	0.01 μF, PTM, 100 V, 1%
C89	285-0596-00	0.01 μF, PTM, 100 V, 1%
C90	281-0525-00	470 pF, Cer, 500 V, 20%
C149	283-0068-00	0.01 μF, Cer, 500 V
C171	283-0068-00	0.01 μF, Cer, 500 V
C174	285-0596-00	0.01 μF, PTM, 100 V, 1%
C175	285-0596-00	0.01 μF, PTM, 100 V, 1%
C176	281-0525-00	470 pF, Cer, 500 V, 20%

CAPACITORS

C201	283-0068-00	0.01 μF, Cer, 500 V
C202	290-0523-00	2.2 μF, Elect., 20 V, 20%
C209	283-0068-00	0.01 μF, Cer, 500 V
C241	283-0000-00	0.001 μF, Cer, 500 V
C276	290-0512-00	22 μF, Elect., 15 V, 20%
C280	290-0512-00	22 μF, Elect., 15 V, 20%
C282	283-0000-00	0.001 μF, Cer, 500 V
C286	283-0000-00	0.001 μF, Cer, 500 V
C301	283-0203-00	0.47 μF, Cer, 50 V, 20%
C329	283-0068-00	0.01 μF, Cer, 500 V
C359	283-0068-00	0.01 μF, Cer, 500 V

DIODES

CR180	152-0141-02	Silicon, selected from 1N4152
CR181	152-0141-02	Silicon, selected from 1N4152
CR182	152-0141-02	Silicon, selected from 1N4152
CR183	152-0141-02	Silicon, selected from 1N4152
CR185	152-0141-02	Silicon, selected from 1N4152
CR186	152-0141-02	Silicon, selected from 1N4152
CR187	152-0141-02	Silicon, selected from 1N4152
CR188	152-0141-02	Silicon, selected from 1N4152
CR189	152-0141-02	Silicon, selected from 1N4152
CR190	152-0141-02	Silicon, selected from 1N4152
CR283	152-0141-02	Silicon, selected from 1N4152
CR285	152-0141-02	Silicon, selected from 1N4152
CR381	152-0141-02	Silicon, selected from 1N4152

DIODES

CR382	152-0141-02	Silicon, selected from 1N4152
CR383	152-0141-02	Silicon, selected from 1N4152
CR384	152-0141-02	Silicon, selected from 1N4152
CR385	152-0141-02	Silicon, selected from 1N4152
CR386	152-0141-02	Silicon, selected from 1N4152
CR387	152-0141-02	Silicon, selected from 1N4152
CR388	152-0141-02	Silicon, selected from 1N4152
CR389	152-0141-02	Silicon, selected from 1N4152

TRANSISTORS

Q77	151-0302-00	Silicon, NPN, replaceable by 2N2222A
Q78	151-0302-00	Silicon, NPN, replaceable by 2N2222A
Q79	151-0188-00	Silicon, PNP, replaceable by 2N3906
Q80	151-1078-00	Silicon, JFET, N channel
Q85	151-1078-00	Silicon, JFET, N channel
Q273	151-1025-00	Silicon, FE, N channel
Q274	151-0410-00	Silicon, PNP, replaceable by 2N5087
Q275	151-0126-00	Silicon, VCDO-45 B-3
Q277	151-0410-00	Silicon, PNP, replaceable by 2N5087
Q278	151-0126-00	Silicon, VCDO-45 B-3

RESISTORS

R29	311-1134-00	50 kΩ, Var
R31	315-0102-00	1 kΩ, 1/4 W, 5%
R39	315-0332-00	3.3 kΩ, 1/4 W, 5%
R72	315-0472-00	4.7 kΩ, 1/4 W, 5%
R73	321-0315-00	18.7 kΩ, 1/8 W, 1%

RESISTORS

R74	321-0289-00	10 kΩ, 1/8 W, 1%
R75	315-0472-00	4.7 kΩ, 1/4 W, 5%
R76	315-0473-00	47 kΩ, 1/4 W, 5%
R77	315-0472-00	4.7 kΩ, 1/4 W, 5%
R83	315-0473-00	47 kΩ, 1/4 W, 5%
R86	308-0697-00	32.140 kΩ, 1/8 W, WW, 1/10%
R87	321-0365-00	61.9 kΩ, 1/8 W, 1%
R88	321-0403-00	154 kΩ, 1/8 W, 1%
R89	321-0365-00	61.9 kΩ, 1/8 W, 1%
R90	315-0106-00	10 MΩ, 1/4 W, 5%
R175	315-0106-00	10 MΩ, 1/4 W, 5%
R176	321-0365-00	61.9 kΩ, 1/8 W, 1%
R177	321-0403-00	154 kΩ, 1/8 W, 1%
R178	321-0365-00	61.9 kΩ, 1/8 W, 1%
R182	308-0698-00	16.046 kΩ, 1/8 W, WW, 1/10%
R183	308-0658-00	4.0 kΩ, 1/8 W, WW, 1/10%
R186	308-0699-00	8.0115 kΩ, 1/8 W, WW, 1/10%
R187	315-0303-00	30 kΩ, 1/4 W, 5%
R191	322-0696-00	128.93 kΩ, 1/4 W, 1%
R192	323-0510-00	2 MΩ, 1/2 W, 1%
R193	322-0693-00	1.036 MΩ, 1/4 W, 1%
R194	322-0694-00	517.1 kΩ, 1/4 W, 1%
R195	322-0697-02	64.374 kΩ, 1/4 W, 1/2%

RESISTORS

R196	322-0695-00	258.2 kΩ, 1/4 W, 1%
R201	315-0102-00	1 kΩ, 1/4 W, 5%
R241	315-0153-00	15 kΩ, 1/4 W, 5%
R261	315-0472-00	4.7 kΩ, 1/4 W, 5%
R264	315-0472-00	4.7 kΩ, 1/4 W, 5%
R265	315-0472-00	4.7 kΩ, 1/4 W, 5%
R273	315-0473-00	47 kΩ, 1/4 W, 5%
R274	321-0315-00	18.7 kΩ, 1/8 W, 1%
R275	321-0289-00	10 kΩ, 1/8 W, 1%
R276	321-0318-00	20 kΩ, 1/8 W, 1%
R277	315-0473-00	47 kΩ, 1/4 W, 5%
R278	315-0303-00	30 kΩ, 1/4 W, 5%
R280	315-0681-00	680 Ω, 1/4 W, 5%
R281	315-0681-00	680 Ω, 1/4 W, 5%
R283	321-0261-00	5.11 kΩ, 1/8 W, 1%
R284	315-0473-00	47 kΩ, 1/4 W, 5%
R285	321-0210-00	1.5 kΩ, 1/8 W, 1%
R286	315-0101-00	100 Ω, 1/4 W, 5%
R287	315-0222-00	2.2 kΩ, 1/4 W, 5%
R288	315-0473-00	47 kΩ, 1/4 W, 5%
R289	321-0272-00	6.65 kΩ, 1/8 W, 1%
R290	321-0221-00	1.96 kΩ, 1/8 W, 1%
R303	315-0472-00	4.7 kΩ, 1/4 W, 5%

RESISTORS

R309	315-0472-00	4.7 kΩ, 1/4 W, 5%
R331	315-0472-00	4.7 kΩ, 1/4 W, 5%
R345	315-0472-00	4.7 kΩ, 1/4 W, 5%
R349	315-0472-00	4.7 kΩ, 1/4 W, 5%
R380	308-0697-00	32.140 kΩ, 1/8 W, WW, 1/10%
R381	308-0698-00	16.046 kΩ, 1/8 W, WW, 1/10%
R382	308-0699-00	8.0115 kΩ, 1/8 W, WW, 1/10%
R387	308-0658-00	4 kΩ, 1/8 W, WW, 1/10%
R391	322-0697-02	64.374 kΩ, 1/4 W, 1/2%
R392	322-0696-00	128.93 kΩ, 1/4 W, 1%
R393	323-0510-00	2 MΩ, 1/2 W, 1%
R394	322-0693-00	1.036 MΩ, 1/4 W, 1%
R395	322-0694-00	517.1 kΩ, 1/4 W, 1%
R396	322-0695-00	258.2 kΩ, 1/4 W, 1%

INTEGRATED CIRCUITS

U9	156-0041-01	Dual 15 MHz D-type pos.-edge-trig., flip-flop, replaceable by SN7474N
U31	156-0172-01	Dual retrig. monostable multivibrators, replaceable by SN74123
U39	156-0039-01	Dual 15 MHz J-K master-slave, flip-flop, replaceable by SN7473N
U41	156-0032-01	Single 10 MHz 1-&-3-bit binary ripple counter, replaceable by SN7493N
U49	156-0061-01	Single bcd to decimal decoder, replaceably by SN7442N
U51	156-0075-01	Single 8-bit data selector/multiplexer, replaceable by SN74151N

INTEGRATED CIRCUITS

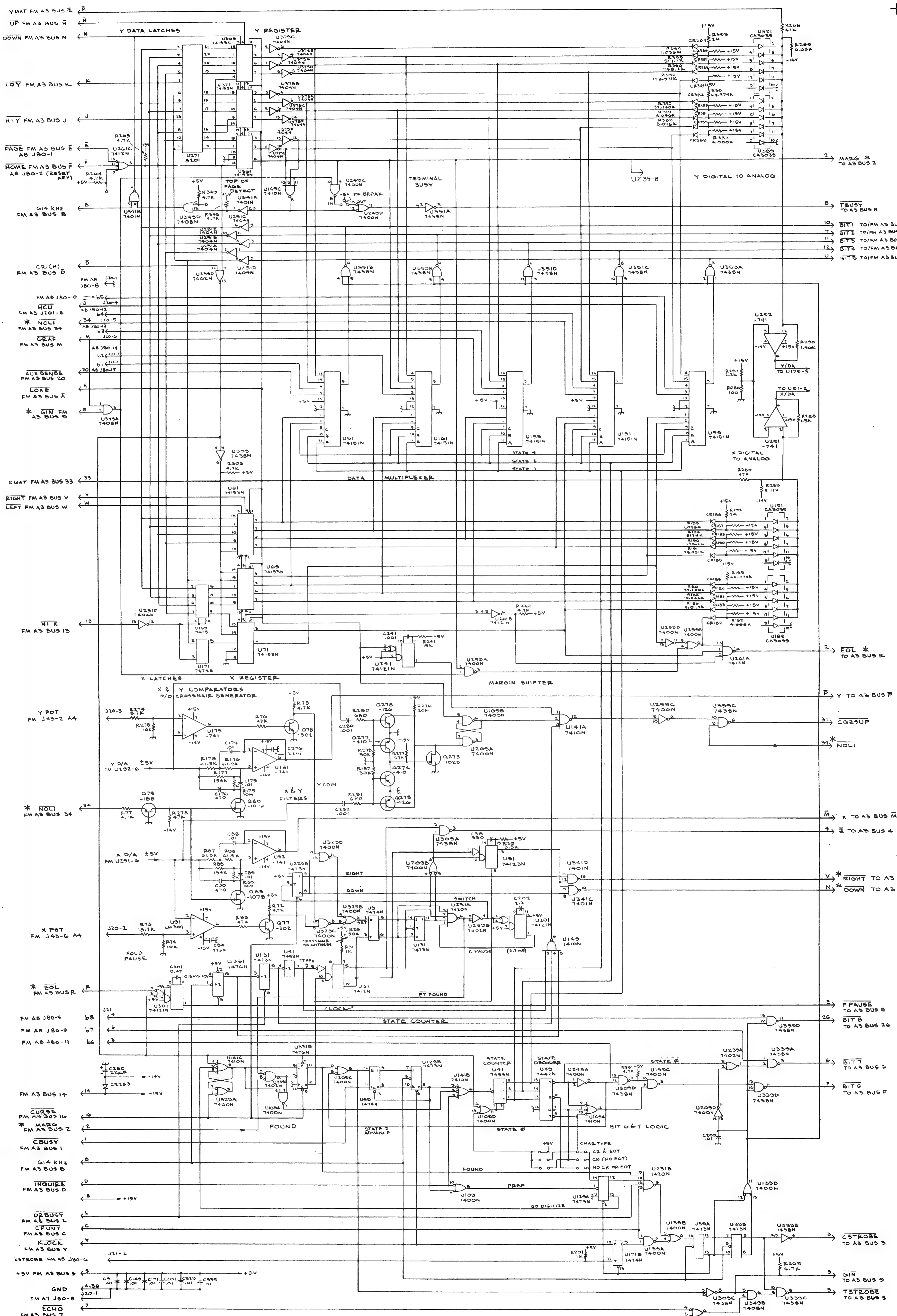
U59	156-0075-01	Single 8-bit data selector/multiplexer, replaceable by SN74151N
U61	156-0089-01	Single 25 MHz sync. 4-bit up/down counter, replaceable by SN74193N
U69	156-0089-01	Single 25 MHz sync. 4-bit up/down counter, replaceable by SN74193N
U71	156-0089-01	Single 25 MHz sync. 4-bit up/down counter, replaceable by SN74193N
U91	156-0105-01	Operational amplifier, replaceable by LM301AN
U92	156-0067-07	Operational amplifier, selected from UA741C
U109	156-0030-01	Quad 2-input positive nand gate, replaceable by SN7400N
U129	156-0039-01	Dual 15 MHz J-K master-slave, flip-flop, replaceable by SN7473N
U131	156-0039-01	Dual 15 MHz J-K master-slave, flip-flop, replaceable by SN7473N
U139	156-0030-01	Quad 2-input positive nand gate, replaceable by SN7400N
U141	156-0047-01	Triple 3-input positive nand gate, replaceable by SN7410N
U149	156-0047-01	Triple 3-input positive nand gate, replaceable by SN7410N
U151	156-0075-01	Single 8-bit data selector/multiplexer, replaceable by SN74151N
U159	156-0075-01	Single 8-bit data selector/multiplexer, replaceable by SN74151N
U161	156-0075-01	Single 8-bit data selector/multiplexer, replaceable by SN74151N
U169	156-0040-01	Dual 2-bit bistable latch, replaceable by SN7475N
U171	156-0041-01	Dual 15 MHz D-type pos.-edge-trig., flip-flop, replaceable by SN7474N
U179	156-0067-07	Operational amplifier, selected from UA741C

INTEGRATED CIRCUITS

U181	156-0067-07	Operational amplifier, selected from UA741C
U189	156-0106-01	Monolithic 6-diode array, replaceable by RCA3039
U191	156-0106-01	Monolithic 6-diode array, replaceable by RCA3039
U201	156-0072-01	Single monostable multivibrator-one shot, replaceable by SN74121N
U209	156-0030-01	Quad 2-input positive nand gate, replaceable by SN7400N
U229	156-0039-01	Dual 15 MHz J-K master-slave, flip-flop, replaceable by SN7473N
U231	156-0034-01	Dual 4-input positive nand gate, replaceable by SN7420N
U239	156-0043-01	Quad 2-input positive nor gate, replaceable by SN7402N
U241	156-0072-01	Single monostable multivibrator-one shot, replaceable by SN74121N
U249	156-0030-01	Quad 2-input positive nand gate, replaceable by SN7400N
U251	156-0058-01	Hex. inverter, replaceable by SN7404N
U259	156-0030-01	Quad 2-input positive nand gate, replaceable by SN7400N
U261	156-0144-01	Triple 3-input positive nand gate, replaceable by SN7412N
U271	156-0152-01	Dual 5-bit buffer register, replaceable by N8201N
U291	156-0067-07	Operational amplifier, selected from UA741C
U292	156-0067-07	Operational amplifier, selected from UA741C
U301	156-0072-01	Single monostable multivibrator-one shot, replaceable by SN74121N
U309	156-0145-01	Quad 2-input positive nand buffer, replaceable by SN7438N
U329	156-0030-01	Quad 2-input positive nand gate, replaceable by SN7400N

INTEGRATED CIRCUITS

U331	156-0042-01	Dual 15 MHz J-K master-slave, flip-flop, replaceable by SN7476N
U339	156-0145-01	Quad 2-input positive nand buffer, replaceable by SN7438N
U341	156-0057-01	Quad 2-input positive nand gate, replaceable by SN7401N
U349	156-0129-01	Quad 2-input positive nand gate, replaceable by SN7408N
U351	156-0145-01	Quad 2-input positive nand buffer,replaceable by SN7438N
U359	156-0145-01	Quad 2-input positive nand buffer, replaceable by SN7438N
U361	156-0089-01	Single 25 MHz sync. 4-bit up/down counter, replaceable by SN74193N
U369	156-0089-01	Single 25 MHz sync. 4-bit up/down counter, replaceable by SN74193N
U371	156-0089-01	Single 25 MHz sync. 4-bit up/down counter, replaceable by SN74193N
U378	156-0058-01	Hex. inverter, replaceable by SN7404N
U379	156-0058-01	Hex. inverter, replaceable by SN7404N
U389	156-0106-01	Monolithic 6-diode array, replaceable by RCA3039
U391	156-0106-01	Monolithic 6-diode array, replaceable by RCA3039



NOTE: ALL F/F CONNECTIONS NOT SHOWN ARE PULLED HIGH

* APPEAR MORE THAN ONCE

M20,689

A2 TC-2 CARD 670-1729-05

TC-2

TEXT CORRECTIONS

Page 4-6, Step 5, line 5; change to read:
Adjust R29 (R85 on boards numbered 670-1729-04 and below), Crosshair Brightness on TC-2 for nonstoring cursor.

Page 4-6, Step 11; change to read:
11. Crosshair Cursor Intensity Check/Adjustment [R29 (R85 on boards numbered 670-1729-04 and below), Crosshair Cursor Brightness on TC-2 in the pedestal].

Adjust R29 (R85 on boards numbered 670-1729-04 and below) in GIN Mode so that the cursor is visible but does not store.

Page 4-14, Fig. 4-7, change "R85 Cross-hair Brightness" to read:
R29 Cross-hair Brightness (R85 on boards numbered 670-1729-04 and below)

Page 4-14, Adjustment 5, Step a, line 4; change to read:
bright, adjust R29 [Crosshair Brightness (R85 on boards numbered 670-1729-04 and below)] on TC-2 as ....

Page 4-19, Fig. 4-12; change "R85 Cross-hair Cursor Brightness" to read:
R29 Cross-hair Cursor Brightness (R85 on boards numbered 670-1729-04 and below).

Page 4-21 Adjustment 11; change to read:
Crosshair Cursor Intensity Check/Adjustment [R29, Crosshair Cursor Brightness on TC-2 (R85 on boards numbered 670-1729-04 and below)]

Page 4-21, Adjustment 11, Step d; change to read:
d. If necessary, adjust R29 (R85 on boards numbered 670-1729-04 and below)--Crosshair Intensity (on TC-2, Fig. 4-12) so that the cursor can be seen.

Page 4-21, Adjustment 11, Step e, line 2; change to read:
stores. Readjust R29 (R85 on boards numbered 670-1729-04 and below) as necessary to provide a clearly..............

Page 6-37, Column 1, line 3; change to read:
75 kHz STEP pulse causes an active Z signal to write (but not store) the point.

Page 6-37, 1st column, 1st para; starting with the 4th sentence, change sentences 4 through 8 to read:

When $\overline{\text{Y}}$ $\overline{\text{COIN}}$ goes low, the Memory Gates output a low $\overline{\text{SET}}$ signal to the Switch Control circuit. FOR TC-2 BOARDS WITH NUMBERS 670-1729-04 AND LOWER, THE FOLLOWING OCCURS: The next $\overline{\text{Q}}$ CLOCK pulse clocks the low $\overline{\text{SET}}$ signal into the Switch Control circuit, causing the $\overline{\text{STEP INH}}$ signal to U67D to go low. This inhibits further STEP pulses that were activating $\overline{\text{DOWN}}$ and $\overline{\text{Z}}$ signals. On the next positive going Q CLOCK pulse, the $\overline{\text{SWITCH}}$ signal goes high. When the positive portion of the Q CLOCK pulse ends, the $\overline{\text{SWITCH}}$ signal goes low, putting a low on the DOWN line and a high on the RIGHT line. FOR TC-2 BOARDS WITH NUMBERS 670-1729-05 AND UP, THE FOLLOWING OCCURS: When $\overline{\text{Y}}$ $\overline{\text{COIN}}$ goes low, the Memory Gates output a low $\overline{\text{SET}}$ signal to the Switch Control circuit. The next $\overline{\text{STEP}}$ pulse clocks the low set signal into the Switch Control Circuit, which enables the $\overline{\text{INHIBIT}}$ signal. $\overline{\text{INHIBIT}}$ prevents further $\overline{\text{STEP}}$ signals from activating $\overline{\text{DOWN}}$ and $\overline{\text{Z}}$ signals. On the next positive-going STEP pulse, the $\overline{\text{SWITCH}}$ signal goes high. When the positive portion of the STEP signal ends, the $\overline{\text{SWITCH}}$ signal goes low, putting a low on the DOWN line and a high on the RIGHT line. THIS ENDS DIFFERENCES IN CIRCUIT OPERATION FOR THIS PARAGRAPH.

Page 6-37; change the 2nd paragraph to read:

FOR TC-2 BOARD NUMBERS 670-1729-04 AND LOWER: The end of the high Q CLOCK pulse also causes the $\overline{\text{STEP INH}}$ signal to U67D to go high. Once again, U67D outputs STEP pulses to the Axis Switching circuit. This time the $\overline{\text{RIGHT}}$ line is being pulsed because of the high on the RIGHT line.

FOR TC-2 BOARD NUMBERS 670-1729-05 AND UP: The end of the high STEP pulse also causes the $\overline{\text{INHIBIT}}$ signal to U309A and Axis Switching circuit to go high. Once again U309A begins outputting active $\overline{\text{Z}}$ signals. Also, with $\overline{\text{INHIBIT}}$ high, the $\overline{\text{RIGHT}}$ line can be pulsed because of the high on the RIGHT line.

Page 6-37; change the first sentence of the third paragraph to read:

FOR TC-2 BOARD NUMBERS 670-1729-04 AND LOWER: With U67D enabled, the clock circuit sends out pulses through U67D to generate $\overline{\text{Z}}$ and $\overline{\text{RIGHT}}$

signals until the X Register reaches or slightly passes the value selected by the X Position Pot.

FOR TC-2 BOARD NUMBERS 670-1729-05 AND UP: With U309A enabled, STEP pulses the $\overline{Z}$ line until the X Register reaches or slightly passes the value selected by the X Position Pot.

Fig. 6-9 Change cutline to read:
Graphic Modes Block Diagram (for boards with numbers 670-1729-04 and lower).

Fig. 6-18 Change cutline to read:
TC-2 Detailed Block Diagram (for boards with numbers 670-1729-04 and lower).

Fig. 6-18A Add:
Fig. 6-18A. TC-2 Detailed Block Diagram (for boards numbered 670-1729-05 and up) A new Fig. 6-18A is attached.

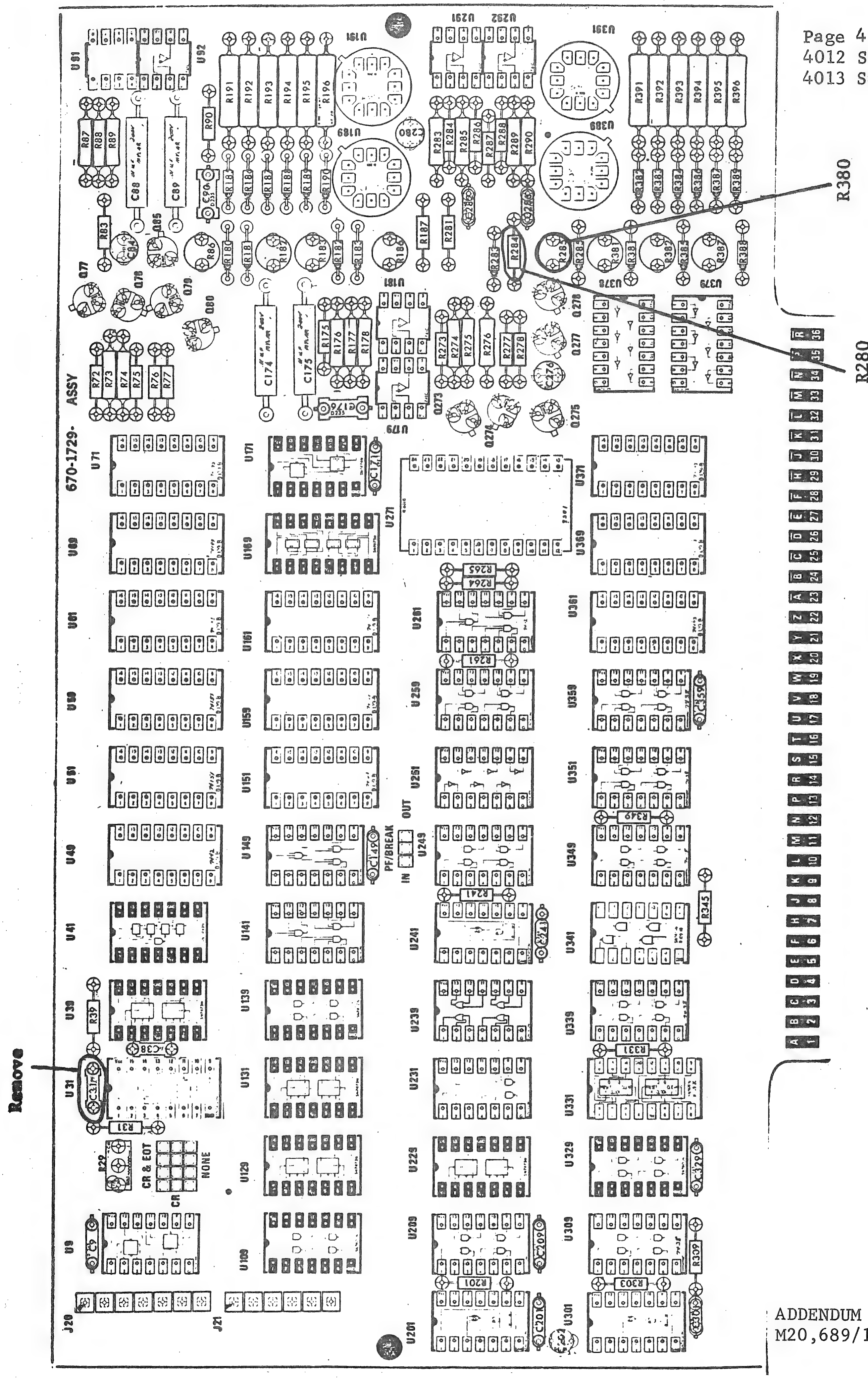
Fig. 6-19 Change cutline to read:
TC-2 Component Locations (for boards numbered 670-1729-04 and lower).

On M20,436/573, page 1 of 6, in the 4th line, change:
670-1729-04 to 670-1729-05.

Fig. 6-19A Add:
TC-2 Component Locations (for boards numbered 670-1729-05 and up).
A new illustration is attached.

Fig. 6-20 Change cutline to read:
TC-2 Schematic (for boards numbered 670-1729-04 and lower).

Fig. 6-20A Add:
TC-2 Schematic (for boards numbered 670-1729-05 and up).
A new schematic was included with M20,689.



TC2 Circuit Card 388-2294-01, Assembly 670-1729-05
(After M20689)

ADDENDUM
M20,689/1173

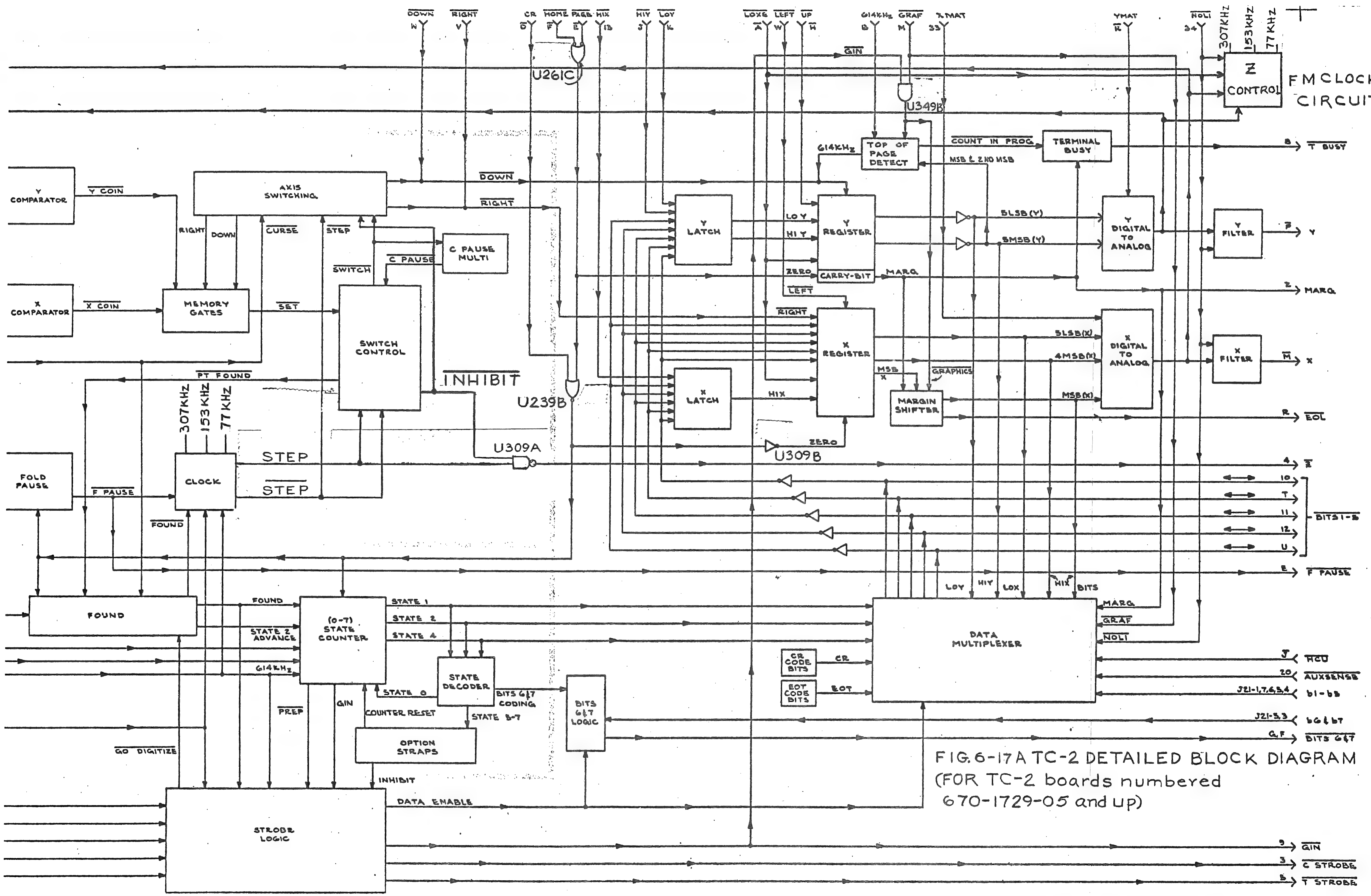


FIG. 6-17A TC-2 DETAILED BLOCK DIAGRAM
(FOR TC-2 boards numbered 670-1729-05 and up)

4012 Service EFF SN B030000-up

ELECTRICAL PARTS LIST AND SCHEMATIC CORRECTION

A1 ASSEMBLY TC-1

CHANGE TO:

A1	670-2372-02	CIRCUIT CARD ASSEMBLY, TC-1

ADD:

CR546	152-0141-02	1N4152
R16	315-0472-00	4.7K ohm, 0.25 W, 5%

MECHANICAL PARTS LIST CORRECTION

Page 7-13

CHANGE TO:

Fig. 4-96	131-0608-00	12	TERMINAL, PIN
	131-0993-00	4	LINK, TERMINAL CONNECTOR

M20,221/873

SCHEMATIC CORRECTION

FIG. 6-31 should read: STORAGE CIRCUIT DAS BOARD #670-2571-04

FIG. 6-31A should read: STORAGE CIRCUIT DAS BOARD #670-2571-03 & below

FIG. 6-34 should read: HARD COPY SELECTOR DAS BOARD #670-2571-04

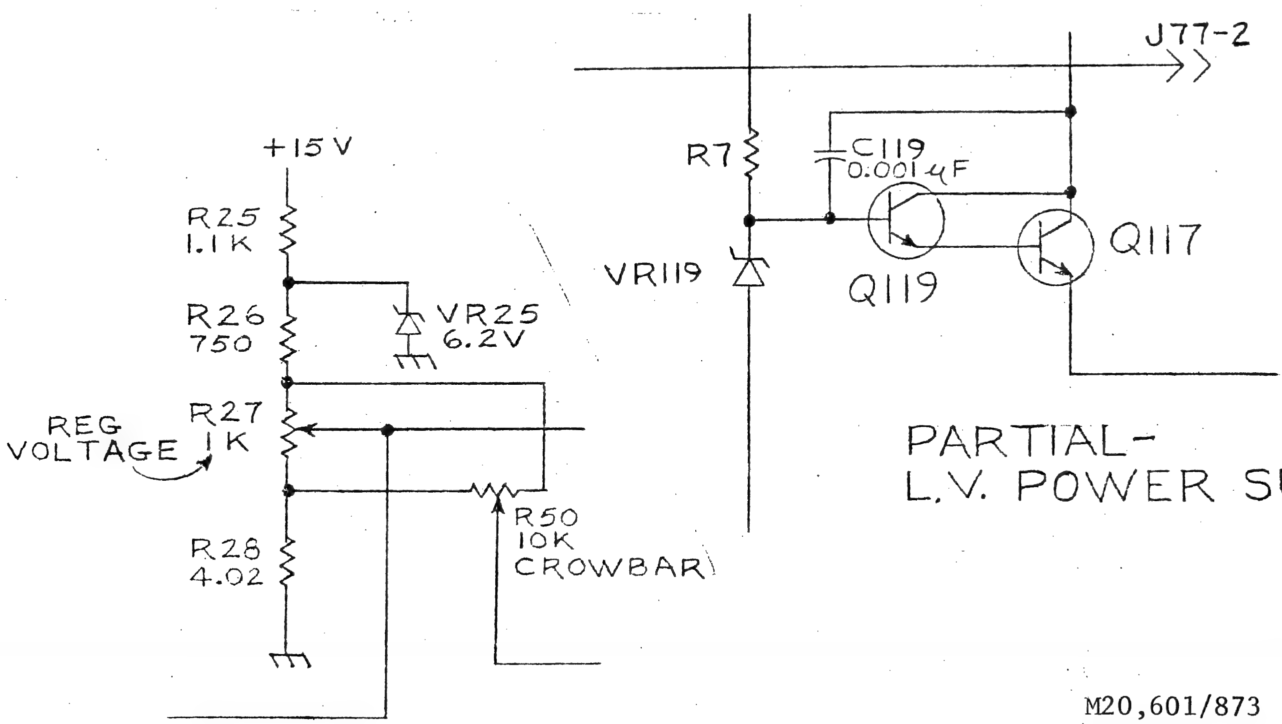
FIG. 6-34A should read: HARD COPY SELECTOR DAS BOARD #670-2571-03 & below

DEFLECTION AMPLIFIERS SCHEMATIC

ADD: C114 between the base and the collector of Q114.

M20,751/873

LOW VOLTAGE POWER SUPPLY corrections as shown below:



PARTIAL-
L.V. POWER SUPPLY

M20,601/873 M20,221
M20,751

4012 Service EFF SN B040000-up

4013 Service EFF SN B040000-up

ELECTRICAL PARTS LIST CHANGE

DISPLAY UNIT CHASSIS

CHANGE TO:

ELECTRON TUBE

V1	154-0624-01	CRT

M21,152/174

4010 Maintenance, 4010-1 Maintenance

4012 Service

4013 Service

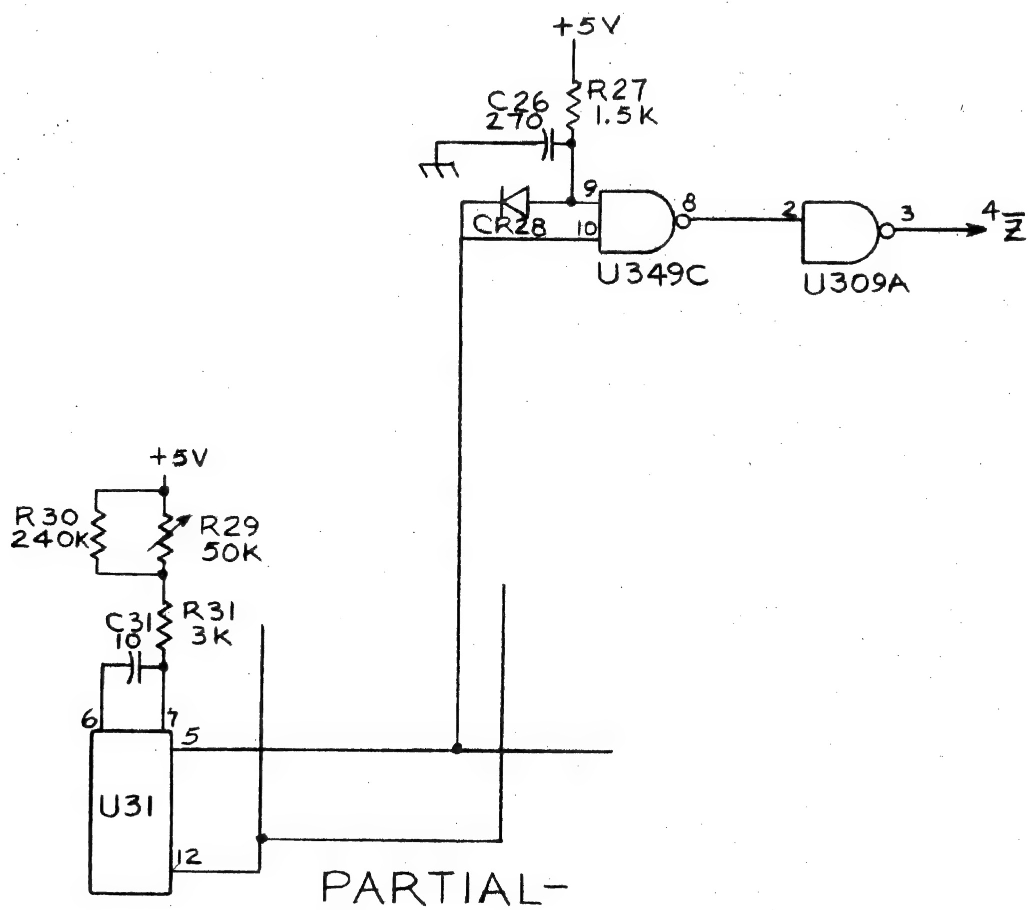
ELECTRICAL PARTS LIST AND SCHEMATIC CHANGE

CHANGE TO:

A2	670-1729-06	CIRCUIT BOARD ASSEMBLY, TC-2
R31	315-0302-00	3 kΩ, 1/4 W, 5%

ADD:

C26	281-0543-00	270 pF, 500 V, ±10%
C31	281-0504-00	10 pF, 500 V, ±1%
CR28	152-0075-00	22 PIV, 40 mA
R27	315-0152-00	1.5 kΩ, 1/4 W, 5%
R30	315-0244-00	240 kΩ, 1/4 W, 5%



PARTIAL-
TC-2 670-1729-06

4010/R, 4010-1/R

4012/R, 4013/R

EFF for 670-1729-07

ELECTRICAL PARTS LIST AND SCHEMATIC CHANGE

A2 ASSEMBLY TC-2

CHANGE TO:

A2	670-1729-07	TC-2 Circuit Card Assembly
R90	315-0396-00	39 MΩ, 1/4 W, 5%
R175	315-0396-00	39 MΩ, 1/4 W, 5%

ELECTRICAL PARTS LIST AND SCHEMATIC CHANGE

CHANGE TO:

ASSEMBLY A4	670-2571-05	DEFLECTION AMPL & STORAGE Circuit Board Assembly
R107	315-0271-00	270 ohm, 0.25 W, 5%
R136	301-0102-00	1K ohm, 0.50 W, 5%
R137	315-0271-00	270 ohm, 0.25 W, 5%
VR135	152-0278-00	1N4372A, 0.4W, 3V

ADD:

CR421	152-0141-02	1N4152
CR422	152-0141-02	1N4152
CR423	152-0141-02	1N4152
CR424	152-0141-02	1N4152

M20,807/174

CHANGE TO:

ASSEMBLY A4	670-2571-06	DEFLECTION AMPL & STORAGE Circuit Board Assembly
C271	283-0111-00	0.1μF, Cer, 50V, 20%
C476	283-0013-00	0.01μF, Cer, 1000V
C585	283-0013-00	0.01μF, Cer, 1000V
C595	283-0013-00	0.01μF, Cer, 1000V
C674	283-0013-00	0.01μF, Cer, 1000V
C675	283-0013-00	0.01μF, Cer, 1000V
C680	283-0013-00	0.01μF, Cer, 1000V
CR695	152-0107-00	TI60 or 1N647

M20,807/174
M21,528/174

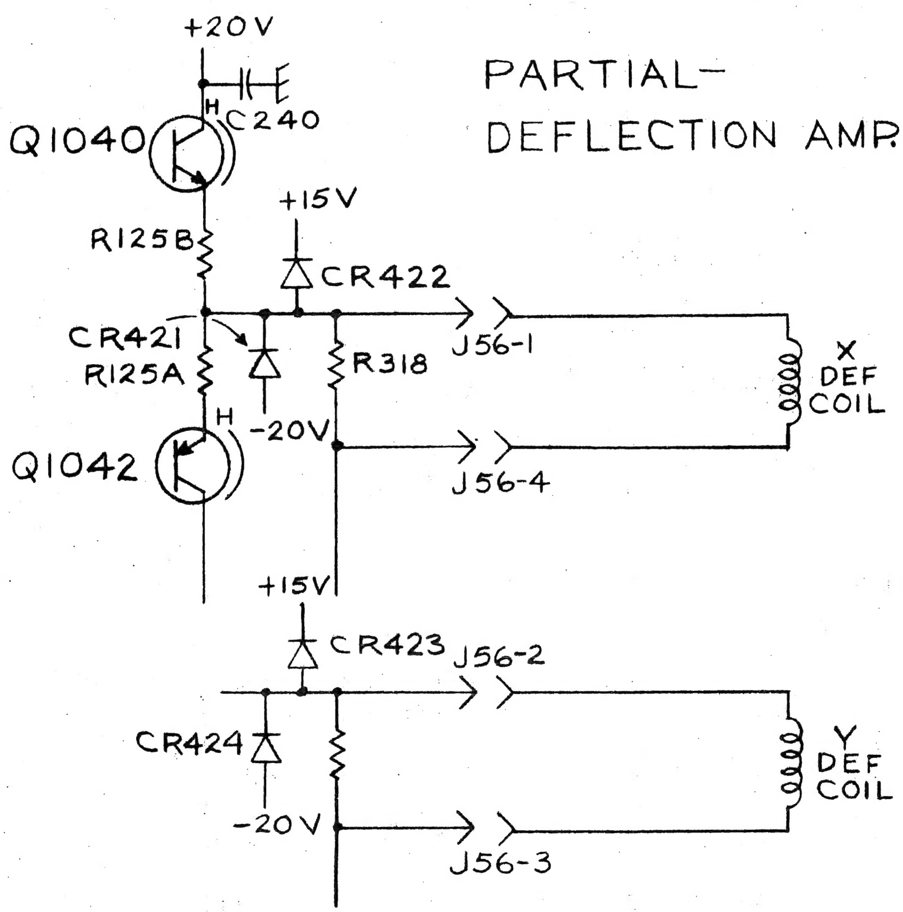
CHANGE TO:

Q568	151-0169-00	SILICON, NPN 2N3439
R566	315-0392-00	3.9K OHM, 0.25W, 5%
R567	315-0682-00	6.8K OHM, 0.25W, 5%

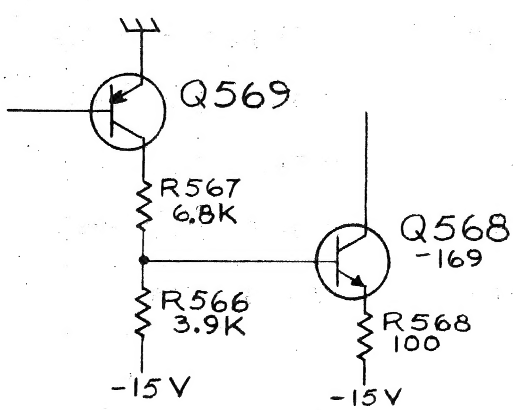
ADD:

R568	315-0101-00	100 OHM, 0.25W, 5%

M21,528



PARTIAL-
DEFLECTION AMP.



PARTIAL-
STORAGE BOARD

M20,807/174
M21,528/174

TEKTRONIX®
committed to technical excellence

MANUAL CHANGE INFORMATION

PRODUCT 4012/R, 4013/R
670-2521-02

CHANGE REFERENCE M21,694
DATE 4-19-74

CHANGE:	DESCRIPTION

ELECTRICAL PARTS LIST AND SCHEMATIC CHANGES

CHANGE TO:

A6	670-2521-02	HV & Z AXIS Circuit Board Assembly
R47	315-0102-03	1K ohm, 0.25W, 5% (Allen/Bradley)
R55	315-0102-03	1K ohm, 0.25W, 5% (Allen/Bradley)
R187	315-0102-03	1K ohm, 0.25W, 5% (Allen/Bradley)
R269	315-0470-03	47 ohm, 0.25W, 5% (Allen/Bradley)
R281	315-0102-03	1K ohm, 0.25W, 5% (Allen/Bradley)
R287	315-0102-03	1K ohm, 0.25W, 5% (Allen/Bradley)
R346	315-0102-03	1K ohm, 0.25W, 5% (Allen/Bradley)
R381	315-0102-03	1K ohm, 0.25W, 5% (Allen/Bradley)